उद्यमेन हि सिध्यन्ति
कार्याणि न मनोरथैः

MAHARAJA AGRASEN INSTITUTE OF TECHNOLOGY

Approved by AICTE Ministry of HRD, Government of India and
Affiliated to Guru Gobind Singh Indraprastha University, Delhi

DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

TECHVOLVE

(2024-25)

(TECHNICAL MAGAZINE)

UNVEILING THE POWER OF CIRCUITS AND WAVES

Maharaja Agarasen Chowk,PSP Area, Sector -22 Rohini New Delhi86
www.ece.mait.ac.in

Maharaja Agrasen Institute of Technology

(Department of Electronics and Communication Engineering)

VISION

To excel in technical education, research, and development across diverse domains of Electronics and Communication Engineering developing entrepreneurs and ethical technocrats.

MISSION

M1: To provide advanced education in Electronics and Communication Engineering, inspiring lifelong learning and academic growth.

M2: To collaborate with industry to develop skilled professionals with ethical and social values.

M3: To enrich teaching by blending traditional methods with evolving digital resources while promoting research, innovation and entrepreneurship.

M4: To encourage teamwork and engage stakeholders in fostering overall development.

Maharaja Agrasen Institute of Technology

(Department of Electronics and Communication Engineering)

PROGRAM EDUCATIONAL OBJECTIVES (PEOs)

PEO1. Graduates will excel in industry, technical professions, higher education and research.

PEO2. Graduates will analyze real life problems and design feasible, socially acceptable systems.

PEO3. Graduates will embrace lifelong learning, ethics and leadership to resolve global challenges.

PEO4. Graduates will develop teamwork, entrepreneurship and a multidisciplinary outlook.

PROGRAM SPECIFIC OUTCOMES (PSOs)

PSO1: Apply Electronics & Communication knowledge to excel in research, industry and entrepreneurship.

PSO2: Innovate and solve complex problems using advanced semiconductor, communication, IoT, embedded and signal processing technologies.

PSO3: Utilize electronics hardware and software tools to address societal challenges.

Maharaja Agarsen Institute of Technology

(Department of Electronics and Communication Engineering)

Message from the Head of the Department

It is a moment of immense satisfaction to introduce the 2024–25 edition of *TECHVOLVE*, the annual technical magazine of our Department of Electronics and Communication Engineering. This magazine is not merely a collection of articles; it is a celebration of imagination, intellect, and innovation. Each page reflects the passion of our students and faculty for exploring new ideas, pushing boundaries, and contributing to the ever-evolving world of technology. The year 2024–25 has been one of growth and achievement for our department. Our students have excelled not only in academics but also in research and technical events, bringing laurels at prestigious forums. We have expanded our horizons into cutting-edge areas such as semiconductor technologies, VLSI system design, 5G and beyond, IoT solutions, AI-driven communication systems, and nanotechnology-based applications. Collaborations with industry and research institutions have further enriched our learning environment, ensuring that our students gain the skills and perspective needed for a dynamic professional world. This edition of *TECHVOLVE* captures the essence of our journey, where knowledge meets creativity, and aspirations turn into tangible outcomes. I commend the editorial team, authors, and mentors who have worked with dedication to make this publication a reality.

As we look to the future, I encourage our budding engineers to nurture curiosity, embrace innovation fearlessly, and commit themselves to using technology for the betterment of society. May *TECHVOLVE 2024–25* continue to inspire minds, spark meaningful discussions, and serve as a beacon of the spirit that defines the ECE fraternity.

With warm regards,

Dr. Sunil Kumar
Head of Department, ECE

Maharaja Agrasen Institute of Technology
(Department of Electronics and Communication Engineering)

Table of Content

Sr. No.	Title	Page No.
1	**Embedded Systems and Their Applications** *Ms. Abhilasha Gokhale, Assistant Professor, Department of Electronics and Communication Engineering, Students: Gunan Jain (20314802821), Saswati Krishnan (23714802821) and Ashwani Kumar (12814802821)*	1
2	**Analyzing the Dual-Metal Junctionless Nanotube Field-Effect Transistors for high Temperature Performances** *Dr. Anubha Goel, Assistant Professor, Department of Electronics and Communication Engineering, Students: Anupam Anand, Vasu Bansal, Pranav Bansal*	6
3	**Silicon Carbide-Based Dielectric Modulated Triple Metal Gate All-Around MOSFET for Enhanced Electrical Characteristics And Analog Performance** *Ms.Neeraj, Assistant Professor, Department of Electronics and Communication Engineering, Students: Ms. Neeti Mishra(07914802821) and Ms.Neha Mishra(07814802821)*	15
4	**Satellite Image Processing** *Mr. Rohit Uday Lakhane, Assistant Professor, Department of Electronics and Communication Engineering, Students: Vansh Kalra (02914802821), Prajwal Khandelwal(03014802821), Lakshya Narang (07414802821)*	21
5	**Next-Gen Gas Detection: A Junctionless Nanowire Ferroelectric FET for PH_3 Sensing** *Faculty: Shalu Garg, Assistant Professor, Department of Electronics and Communication Engineering, Student: Anurag Rungta (21114802822), Sandhya Tiwari (21514802822)*	30
6	**Blood Cancer & Leukemia Identification Using Hybrid Ensemble Deep Learning** *Prof. (Dr.) Sunil Kumar, HOD, Department of Electronics and Communication, Engineering, Students: Raghav Gupta, Akshat Bhardwaj, Varun Sharma*	32

Embedded Systems and Their Applications

Ms. Abhilasha Gokhale, Assistant Professor, Department of Electronics and Communication Engineering, Students: Gunan Jain (20314802821), Saswati Krishnan (23714802821) and Ashwani Kumar (12814802821)

INTRODUCTION

Embedded systems represent a cornerstone in modern digital technology, offering tailored solutions for dedicated tasks within larger electrical or mechanical systems.[1] The reduction in microprocessor and memory component size, accompanied by increased computational efficiency, has allowed embedded systems to become deeply integrated into a diverse range of real-time applications. These systems are typically composed of a microcontroller or microprocessor, memory, input/output interfaces, and software configured to perform a specific function reliably and efficiently. Unlike general-purpose computing devices, embedded systems operate under strict performance, power, and time constraints, which makes their design a subject of extensive research and optimization.

The critical aspect of embedded system design lies in the balance between hardware resources and software functionality. The interaction between these two domains is expressed mathematically through performance evaluation models that consider execution time, power consumption, and memory usage. One such model is defined as:

In Equation 1, represents the power consumption, the energy consumed, and the

$$P = \frac{E}{T} = V^2 \cdot f \cdot C \quad (1)$$

time of operation. The right-hand side of the equation derives from dynamic power dissipation theory, where denotes the supply voltage, the operating frequency, and the switching capacitance. This equation becomes central when optimizing embedded hardware for battery-powered applications such as IoT devices, wearables, and portable medical equipment.[2]

Another essential performance metric is system latency, often modeled as:

$$L = D + \frac{Q}{B} \quad (2)$$

Where denotes latency, is the propagation delay, is the queue length, and is the bandwidth. This expression is vital for networked embedded systems, ensuring predictable response times.

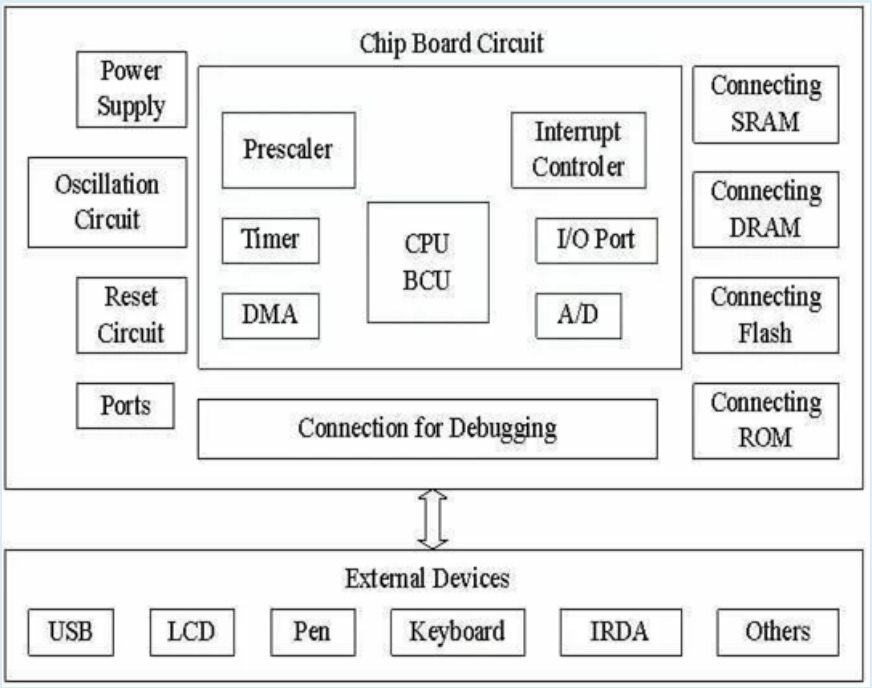
For real-time systems, schedulability is determined by utilization bounds:

$$U = \sum_{i=1}^{n} \frac{C_i}{T_i} \leq 1 \quad (3)$$

Here, is processor utilization, is computation time of task , and is its deadline. For Rate Monotonic Scheduling (RMS), the bound becomes:

$$U \leq n(2^{1/n} - 1) \quad (4)$$

DEVICE STRUCTURE



The above image illustrates the fundamental architecture of a typical embedded system, highlighting both internal components and interfaces with external devices.[3] At the center of the architecture is the System Core, typically comprising a Central Processing Unit (CPU) or Base Control Unit (BCU), responsible for executing control algorithms and managing system operations. Surrounding the core are key functional modules such as Timers, Direct Memory Access (DMA) controllers, and Prescalers, which facilitate accurate timing, efficient data transfer, and system synchronization.

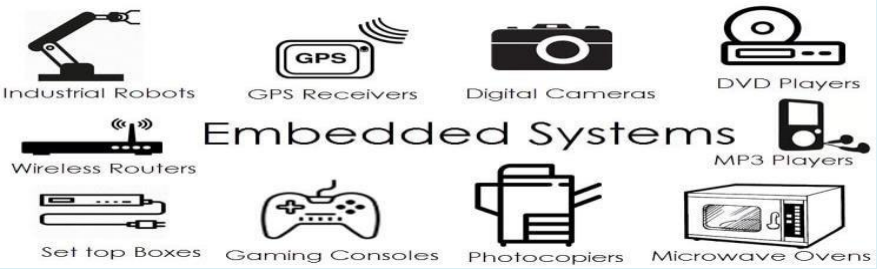
An Interrupt Controller is integrated to prioritize and manage real-time tasks, enabling responsive system behavior under time-critical conditions. The system also includes Analog- to-Digital (A/D) Converters and Input/Output (I/O) Ports, which support signal conditioning and communication with sensors, actuators, and other external devices. Memory interfacing is achieved through connections to Static RAM (SRAM), Dynamic RAM (DRAM), Flash Memory, and Read-Only Memory (ROM), thereby offering both volatile and non-volatile storage capabilities.

Peripheral subsystems such as the Oscillation Circuit, Reset Circuit, and Power Supply Unit ensure stable and continuous system operation under varying environmental conditions. A dedicated Debugging Interface provides real-time system monitoring and supports diagnostic operations during the development and testing phases. Furthermore, the architecture accommodates communication with various external peripherals, including USB devices, LCD panels,keyboards, and infrared data modules (IRDA), thereby demonstrating its adaptability and broad application scope in embedded environments..

CLASSIFICATION OF EMBEDDED SYSTEMS

Embedded systems can be systematically classified based on their performance and functional characteristics into several categories. Real-Time Embedded Systems are designed to perform dedicated tasks within strict timing constraints, where delayed responses can lead to system failure; examples include automotive engine control units and industrial automation systems. Standalone Embedded Systems operate independently and do not require connectivity with a host system or network for execution; typical applications include microwave ovens, washing machines, and digital cameras.[4] Networked embedded systems are integrated with communication interfaces that allow them to exchange data with other systems over wired or wireless networks. They are commonly used in applications such as smart meters, distributed sensor networks, and Internet of Things (IoT) devices. Finally, Mobile Embedded Systems are characterized by their compact, portable design and reliance on battery power, enabling mobility and on-the-go functionality; examples include smartphones, GPS devices, and wearable health monitors. This classification aids in understanding the operational context and design requirements of various embedded applications.

APPLICATIONS OF EMBEDDED SYSTEMS



Embedded systems have become ubiquitous across numerous domains due to their versatility, reliability, and power efficiency. In the automotive sector, they manage essential components such as Engine Control Units (ECUs), Anti-lock Braking Systems (ABS), airbags, and infotainment systems. Consumer electronics rely on embedded controllers in smart TVs, washing machines, and digital cameras. In the medical field, embedded systems are critical for devices like pacemakers, portable diagnostic tools, and wearable health monitors. Industrial automation employs embedded platforms for robotics, sensor networks, and Programmable Logic Controllers (PLCs). Aerospace and defense systems use them for navigation, missile guidance, and flight control.[5] Additionally, the rise of the Internet of Things (IoT) has accelerated embedded integration in smart homes, environmental monitoring, and smart agriculture, driving innovations in connected technologies. Each of these domains benefits from the compact size, high reliability, and low power consumption of embedded systems. Furthermore, as system complexity increases, mathematical models such as Worst-Case Execution Time (WCET):

$$WCET = \max_{\forall i}(T_{execution})_i \quad (5)$$

are crucial for guaranteeing time-bounded operations, especially in safety-critical applications.

CONCLUSION

In conclusion, embedded systems form the backbone of contemporary electronic and automated solutions, offering a harmonious blend of reliability, energy efficiency, and real-time responsiveness. Their integration across diverse sectors—from automotive and healthcare to industrial automation and consumer electronics—underscores their critical role in modern engineering. As

technologies such as Artificial Intelligence (AI) and the Internet of Things (IoT) continue to evolve, embedded systems are poised to become even more intelligent, interconnected, and autonomous. These advancements not only expand the functional landscape of embedded applications but also introduce new challenges in system design, optimization, and security. Therefore, embedded systems remain a dynamic and foundational domain, demanding continuous innovation and expertise from future engineers to meet emerging application requirements and performance benchmarks.

REFERENCES

[1] *Raj Kamal, "Embedded Systems: Architecture, Programming and Design", Tata McGraw Hill, 3rd Edition, 2020.*

[2] *Wayne Wolf, "Computers as Components: Principles of Embedded Computing System Design", Morgan Kaufmann, 2nd Edition.*

[3] *https://www.electronicshub.org/embedded-systems-basics/*

[4] *https://www.electronicshub.org/embedded-systems-applications/*

[5] *https://www.einfochips.com/blog/embedded-systems-in-automotive-industry/*

Analyzing the Dual-Metal Junctionless Nanotube Field-Effect Transistors for high Temperature Performances

Dr. Anubha Goel, Assistant Professor, Department of Electronics and Communication Engineering, Students: Anupam Anand, Vasu Bansal, Pranav Bansal

I. INTRODUCTION

The Metal-Oxide-Semiconductor Field-Effect Transistors (MOSFETs), since its invention in 1959, has been widely used as a primary transistor device and has undergone significant evolution. This evolution has driven advances in the fabrication technology as well as device architecture. The development of various FET architectures like FinFETs[1], Gate all around (GAA) FETs[2], Nanowire[3], [4] and Nanotube[5] transistors as the device is scaled down is the evolution. The continued miniaturization of semiconductor devices for Ultra-Large-Scale Integration (ULSI) has led to the development of novel transistor architectures like Dual Metal Junctionless Nanotube Field Effect Transistors (DMJN-TFETs). These devices offer promising improvements in analog and digital applications, particularly in mitigating short-channel effects (SCEs) and reducing noise. It has already been showed that DMJN-TFETs gives enhanced results over the existing junctionless architectures by giving superior drain current (I_{ds}), transconductance (g_m), output conductance (g_d) and cut-off frequency (f_T). Results have also showed near ideal I_{ON}/I_{OFF} and Subthreshold Slope (SS) for DMJN-TFET[6]. However, in real-world applications, electronic devices often operate under a wide range of temperatures. By changing the temperature of the device operation, one can induce variations in various device parameters (like V_{th}, mobility, leakage current, etc). These variations in device parameters may lead to changing the device performance. Thus, it becomes crucial to analyse the temperature dependent behaviour of DMJN-TFET for assessing their applicability in various thermal environments. While various studies have examined temperature effects on different FET devices, comprehensive thermal analyses for DMJN-TFETs are limited. The goal of this work is to explore how temperature affects the DMJN-TFET's electrical parameters, providing a comprehensive understanding of the device's thermal stability and performance variations. This study focuses on analyzing key parameters such as the drain current (I_{ds}), transconductance (g_m), output conductance(g_d), threshold voltage (V_{th}), and Subthreshold Slope (S_s) across different temperature settings.

II. DEVICE STRUCTURE AND SIMULATION SETUP

The DMJN-TFET consists of:

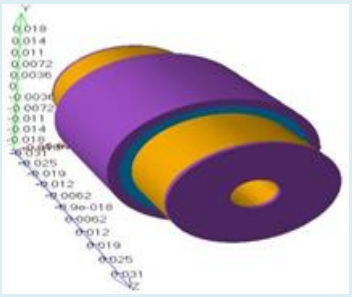
- A cylindrical nanotube channel, in tubular form with junctionless characteristics.
- Two dual metal gates (outer gate and inner gate) for controlling the channel electrostatics and varying the threshold voltage.
- An oxide layer (SiO_2) for isolating the channel and gates.
- Source and drain electrodes at ends of channel which helps to study how charge flows at either side.

A cylindrical silicone geometry of length 60 nm and radius 10 nm is carefully selected with channel length of 30 nm in order to get an optimal gate control and current drive over the channel. The cylindrical geometry provides a higher surface area than other conventional rectangular or planar channels so that wrap around gate can be used to achieve higher electrostatic control.

The dual metal gate structure in DMJN-TFET which uses two distinct metals with work functions of 5.25 eV and 4.75eV utilized in the inner and outer gate cores, allows greater electrostatic control over the channel which improves subthreshold slope and diminishes leakage current. The use of dual gate also provides several other benefits like better grip over threshold voltage, mitigating short channel effects (SCE) and flexibility in device optimization.

2nm thick gate oxide (SiO2) layer as a dielectric material between the dual metal gates and channel for insulating the channel and ensuring an appropriate capacitance to maximize gate control is used. A relative permittivity of 3.9 is defined for the SiO2 layer. It is necessary to opt a carefully picked dielectric value in order to get an optimal gate-channel coupling strength.

The n-type source and drain regions uniformly doped to a concentration of 1019 cm-3, designed in a shape of an annular cylinder is used. The drain and the source electrodes are strategically positioned at the opposite ends of cylindrical nanotube to ensure proper current flow.



(a)

(b)

Fig 1. (a)3D Structure of DMJNTFET (b)Front view

The discussed device was simulated on ATLAS 3D TCAD device simulator to carry out numerical simulations. To account for recombination of electrons and holes through trap states in the bandgap, Shockley-Read-Hall (SRH) recombination model was used. This recombination process is critical for understanding the current flow in the pesented device. Concentration- Dependent Mobility (CONMOB) and Field-Dependent Mobility (FLDMOB) models are used to adjust the carrier mobility in response to doping concentration and high electric field respectively.

The CONMOB captures the effect of increase in carrier scattering with the rise in doping level, leading to reduced carrier mobility. Also, when an electric field in the channel reaches a certain threshold, carriers cannot accelerate indefinitely and reach a saturation velocity, affecting current drive at high bias. This effect is captured under FLDMOB. Moreover, in order to scrutinize carrier statistics, we used Boltzmann Statistics in our device. Together, these options provide a balance between accuracy and computational efficiency while performing device simulations at different temperatures.

Table 1. Device specifications

Parameters	**DMJN-TFET**
Channel length (nm)	L1=15 and L2=15

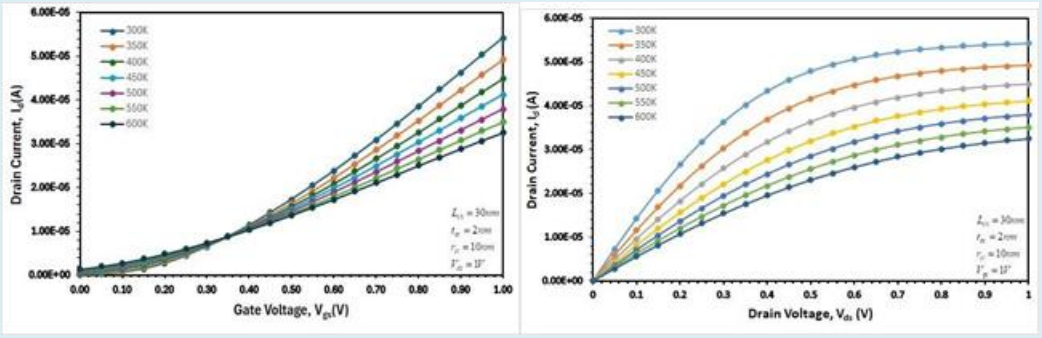
ration of N-Type material in source, drain and channel (cm^{-3})	10^{19}
Work Function of metal contacts (eV)	5.25(Outer), 4.75(Outer), 5.25(Inner), 4.75(Inner)
Thickness of gate-oxide layer (nm)	2
Silicon film radius (nm)	10

III. RESULTS AND DISCUSSION

The following section meticulously scrutinizes the impact of temperature on different device parameters. The parameters in focus are:- drain current (Id), threshold voltage (Vth), subthreshold slope (Ss), transconductance (gm), output conductance (gd) and Ion/Ioff ratio. Previous studies have been conducted on these parameters at room temperature for DMJN-TFET which concluded that the device under consideration performs better on these parameters than other available FETs. So, study of these parameters under varying temperature provides the complete picture of DMJN-TFET as a better alternative, which this study aims to verify.

Fig 2(a) illustrates the variation of Drain current (Id) with Gate Voltage (Vg) across varying temperatures at an interval of 50K. The graph characterizes an increase in off-state current (Ioff) and decrease in on-state current (Ion) with rise in temperature. The graph also becomes less steep as the temperature increases. Elevated temperatures increase intrinsic carrier concentration, leading to a rise in Ioff . As a result, even when Vg is below threshold, the leakage current is higher, and the Ioff increases. Also, higher temperatures increase phonon scattering in the semiconductor lattice, which reduces carrier mobility. This results in a decreased drain current at a given Vg in the on-state (Ion). However, the overall shape of the graph remains consistent with temperature signifying that the conduction process remains unaltered even at temperatures as high as 600K.

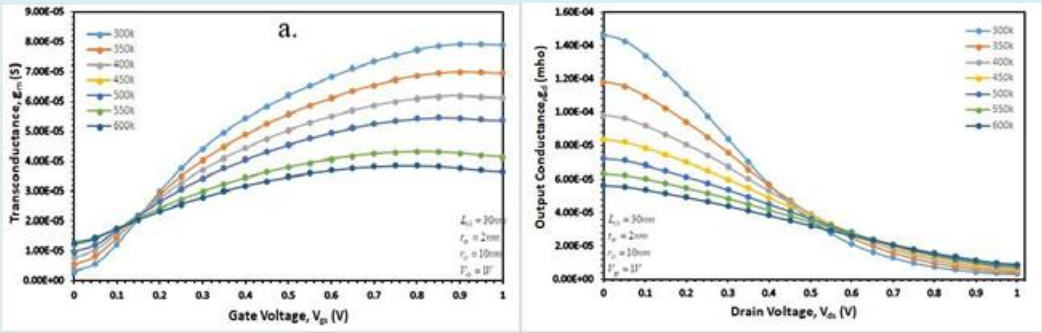
Fig 2(b) shows how the drain current vs gate voltage (Id – Vd characteristics) curve changes with rise in temperature. From the graph, it can be seen that the shape of graph remains unchanged with temperature with a slight decrease in saturation current as the temperature rises. The Id - Vd curve flattens in both the linear and saturation regions due to a combination of reduced mobility, increased leakage, and reduced output conductance.



(a) *(b)*

Fig 2. (a)Id – Vg characteristics and (b) Id – Vd characteristics at different temperatures.

Fig 3(a) and Fig 3(b) shows the transconductance and output conductance at different temperatures. The transconductance (gm) quantifies the change in drain current (Id) resulting from a change in gate voltage (Vg), indicating the efficiency of gate voltage in regulating the drain current. The Fig 3(b) shows that the output conductance also decreases with increase in temperature. This is because higher temperatures lead to earlier channel pinch-off and reduced carrier velocity in the saturation region. Also due to early saturation, Id becomes less sensitive to changes in Vd, leading to a lower gd.



(a) *(b)*

Fig 3. (a)Transconductance(g_m) and (b) Output conductance(g_d) at different temperatures

Fig 4. shows the threshold voltage (V_{th}) of the device across varying temperatures. As observed from the figure, there exists an approximately linear relationship between temperature and the threshold voltage in a junctionless transistor within the temperature range of 300K to 600K. This linear relationship is characterized by a negative slope, i.e. the value of V_{th} decreases almost linearly as the temperature rises. This decrease in V_{th} can be attributed to increase in intrinsic carrier concentration and narrowing of bandgap at higher temperatures.

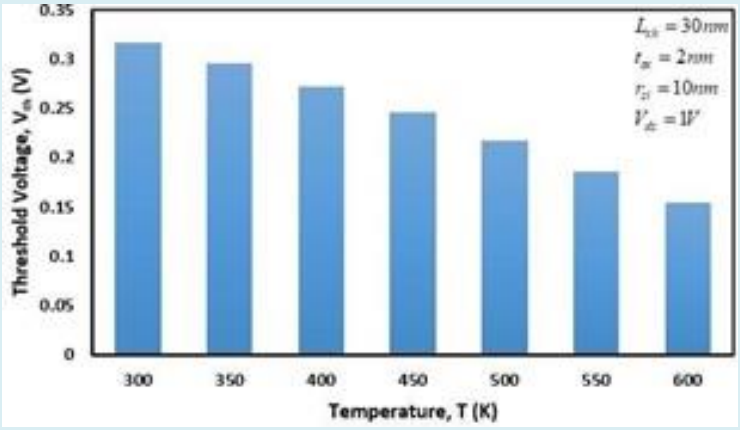


Fig 4. Threshold Voltage of DMJN-TFET at different temperatures

An important parameter that characterizes FET devices is Subthreshold Slope (Ss). It represents the amount of gate voltage required for a tenfold (one order of magnitude) increase the drain current in the subthreshold region, where the transistor is only partially turned on. From equation (6), we can see that the Ss holds a linear relation with temperature. This linear relation is also seen in our simulated model as represented in Fig. 5. The subthreshold slope of DMJN-TFET increases linearly as the temperature is increased.

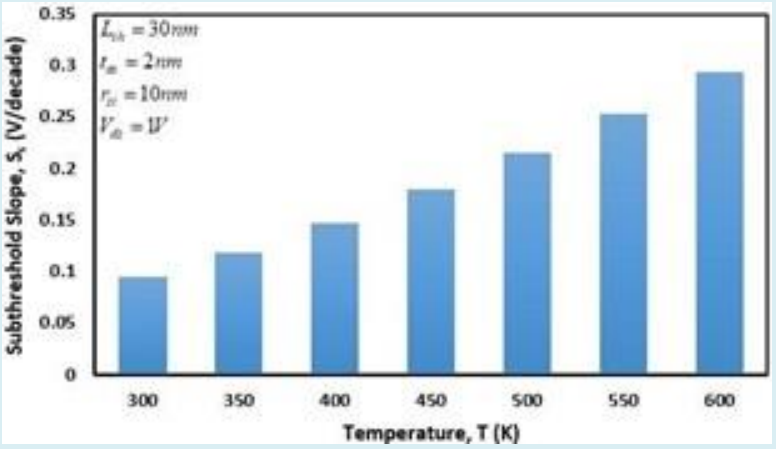


Fig 5. Subthreshold slope of DMJN-TFET at different temperatures

Fig. 6 graphically shows the relationship of Ion/Ioff ratio with temperature. We know that the increase in Ioff is exponential with temperature, driven by the Arrhenius relationship, which makes the off-state leakage very sensitive to temperature changes. Also as discussed earlier the Ion decreases with rise in temperature due to phonon

scattering phenomenon. Thus, the Ion/Ioff ratio should show an exponential decay with temperature. This exponential decay is clearly evident from the fig (6).

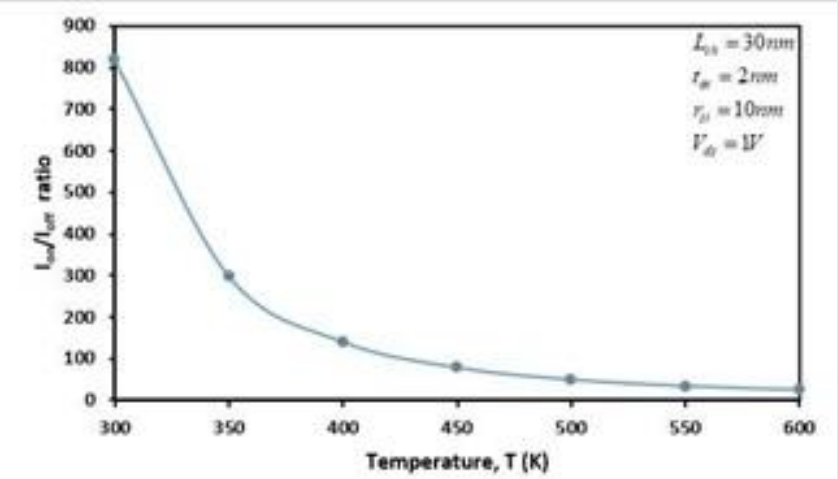


Fig 6. Ion/Ioff vs Temperature curve

IV. CONCLUSION

In conclusion, the findings from our study demonstrate that the Dual-Metal Junctionless Nanotube Field-Effect Transistor (DMJN-TFET) exhibits robust performance across a broad temperature range from 300 K to 600 K. Key device parameters, such as threshold voltage, subthreshold slope, drain current variation with gate voltage and drain voltage, transconductance and output conductance, showed consistent behavior with minimal degradation under increased temperatures. However, the simulation results showed an exponential deterioration of Ion/Ioff ratio with rise in temperature i.e. the Ion/Ioff ratio of the DMJN-TFET decreases exponentially as the working temperature increases.

This deterioration may result in increased delay in device at higher temperatures, reducing its suitability for applications that demand rapid switching under high-temperature conditions. The overall stability across other varying thermal conditions indicates that DMJN-TFETs offer reliable performance, making them advantageous for analog and low-noise applications where thermal resilience is critical. Thus, the DMJN-TFET provides enhanced gate control and superior electrostatic integrity and ensures stable operation over a wide temperature spectrum. Consequently, this study supports the suitability of DMJN-TFETs in high-performance applications where thermal stability and high device reliability are essential requirements.

REFERENCES

[1] *D. Hisamoto et al., "FinFET-A Self-Aligned Double-Gate MOSFET Scalable to 20 nm," 2000.*

[2] *2017 Symposium on VLSI Technology : digest of technical papers : June 5-8, 2017, Kyoto. Japan Society of Applied Physics, 2017.*

[3] *J. P. Colinge et al., "Nanowire transistors without junctions," Nat Nanotechnol, vol. 5, no. 3, pp. 225–229, 2010, doi: 10.1038/nnano.2010.15.*

[4] *L. Mu, Y. Chang, S. D. Sawtelle, M. Wipf, X. Duan, and M. A. Reed, "Silicon nanowire field-effect transistors - A versatile class of potentiometric nanobiosensors," IEEE Access, vol. 3, pp. 287–302, 2015, doi: 10.1109/ACCESS.2015.2422842.*

[5] *"Gate voltage (V):-3 300 K +1 +2 +4 +6 I (nA) 0," 6AD.*

[6] *A. Goel, S. Rewari, S. Verma, and R. S. Gupta, "Novel Dual-Metal Junctionless Nanotube Field-Effect Transistors for Improved Analog and Low-Noise Applications," J Electron Mater, vol. 50, no. 1, pp. 108–119, Jan. 2021, doi: 10.1007/s11664-020-08541-9.*

[7] *A. Nowbahari, A. Roy, and L. Marchetti, "Junctionless transistors: State-of-the-art," Jul. 01, 2020, MDPI AG. doi: 10.3390/electronics9071174.*

[8] *E. Gnani, A. Gnudi, S. Reggiani, and G. Baccarani, "Theory of the junctionless nanowire FET," IEEE Trans Electron Devices, vol. 58, no. 9, pp. 2903–2910, Sep. 2011, doi: 10.1109/TED.2011.2159608.*

[9] *S. Munjal, R. Neelam, P. P. Prakash, and J. Kaur, "Evolution of Junctionless Field Effect Transistors in Semiconductor Industry: A Review," 2021. [Online]. Available: www.ijiset.com*

[10] *A. Talukdar, A. K. Raibaruah, and K. C. Deva Sarma, "Dependence of Electrical Characteristics of Junctionless FET on Body Material," in Procedia Computer Science, Elsevier B.V., 2020, pp. 1046–1053. doi: 10.1016/j.procs.2020.04.112.*

[11] *S. Tayal and A. Nandi, "Study of temperature effect on junctionless Si nanotube FET concerning analog/RF performance," Cryogenics (Guildf), vol. 92, pp. 71–75, Jun. 2018, doi: 10.1016/j.cryogenics.2018.03.012.*

[12] *R. Narang, M. Saxena, R. S. Gupta, and M. Gupta, "Impact of temperature variations on the device and circuit performance of tunnel FET: A simulation study," IEEE Trans Nanotechnol, vol. 12, no. 6, pp. 951–957, 2013, doi: 10.1109/TNANO.2013.2276401.*

[13] *I. A. Pindoo, S. K. Sinha, and S. Chander, "Performance analysis of heterojunction*

tunnel FET device with variable Temperature," Appl Phys A Mater Sci Process, vol. 127, no. 10, Oct. 2021, doi: 10.1007/s00339-021-04891-1.

[14] *2010 IEEE MTT-S International Microwave Symposium : May 23-28, 2010, Anahaeim, California. IEEE, 2010.*

Silicon Carbide-Based Dielectric Modulated Triple Metal Gate All-Around MOSFET for Enhanced Electrical

Characteristics and Analog Performance

Ms. Neeraj, Assistant Professor, Department of Electronics and Communication Engineering, Students: Ms. Neeti Mishra (07914802821) and Ms. Neha Mishra (07814802821)

Abstract

This article presents a novel approach to enhancing the electrical and analog performance of Metal-Oxide- Semiconductor Field-Effect Transistors (MOSFETs) using a Triple Metal Gate All-Around (TMGAA) configuration implemented on a 4H-Silicon Carbide (SiC) substrate. A gate-stack incorporating (high-k) dielectric materials, specifically Hafnium Oxide, HfO_2 and Aluminum Oxide, Al_2O_3, has been utilized as the gate dielectric, the proposed design outperforms the conventional Double Metal Gate All-Around (DMGAA) MOSFET, exhibiting significant improvements in transconductance, drain current, and output conductance. The simulation, performed using the ATLAS 3D device simulator, validates the effectiveness of this structure for high-power, high-frequency, and nanoscale applications.

Introduction

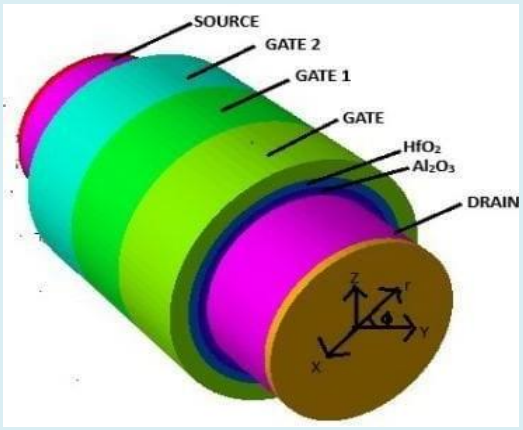
Metal-Oxide-Semiconductor Field-Effect Transistors (MOSFETs) have long been central to the electronics industry, spanning from low-power circuits to high-power applications [1]. Silicon remains the dominant semiconductor material due to its favorable electrical properties and manufacturing compatibility [2]. However, with the push for higher power densities and thermal stability in modern electronics, especially in high-voltage and high-temperature environments, silicon-based MOSFETs show performance limitations such as short- channel effects and high leakage currents [3-4]. Emerging device architectures like the Double Metal Gate (DMGAA) and Triple Metal Gate (TMGAA) MOSFETs have been proposed to mitigate these drawbacks. Silicon Carbide (SiC), particularly the 4H-SiC polytype, offers a wide bandgap of 3.26 eV significantly larger than silicon's 1.1 eV enabling higher breakdown voltages, reduced leakage, and improved thermal conductivity [7-8]. Additionally, Al_2O_3's superior lattice compatibility and thermal properties with SiC make it a preferred dielectric over traditional SiO_2 [9]. When combined with high-k HfO_2 in a

stacked gate dielectric, the device benefits from reduced gate leakage and improved channel control.

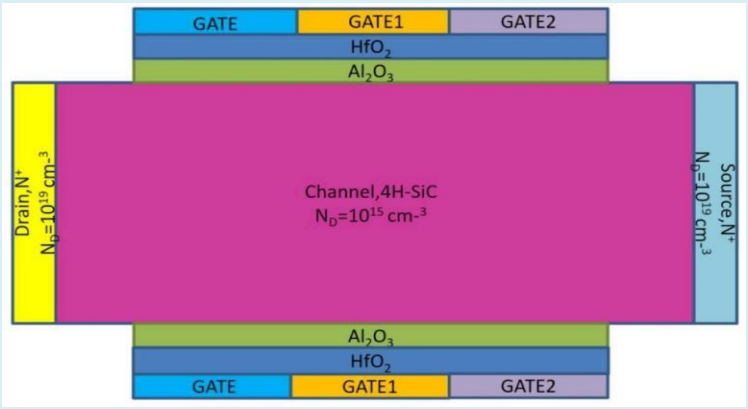
Device Structure

TABLE I DEVICE SPECIFICATIONS FOR A RANGE OF PROPOSED DEVICE DESIGN

Parameters	**DMGAA MOSFET (4H-SiC)**		**TMGAA MOSFET (4H-SiC)**		
Channel Length, L (nm)	L_1	L_2	L_1	L_2	
	25	25	25	25	
Channel Doping ($/cm^3$)	$1x10^{15}$		$1x10^{15}$		
Oxide Thickness (nm)	2	2	2	2	
Silicon/SiC Thickness (nm) t_{si}	10		10		
Gate Work Function (eV)	Φm1 (Niobium)	Φm2 (Boron)	Φm1 (Tungsten)	Φm2 (Vanadium)	Φm3 (Manganese)
	4.85	4.45	4.4	4.3	4.1
Length of S/D (nm)	1		1		



(A)



(B)

Fig. 1 (A) 3-D structure illustration of 4H-SiC-DM-TMGAA-MOSFET. (B) 2-D cross-sectional view of 4H- SiC-DM-TMGAA-MOSFET.

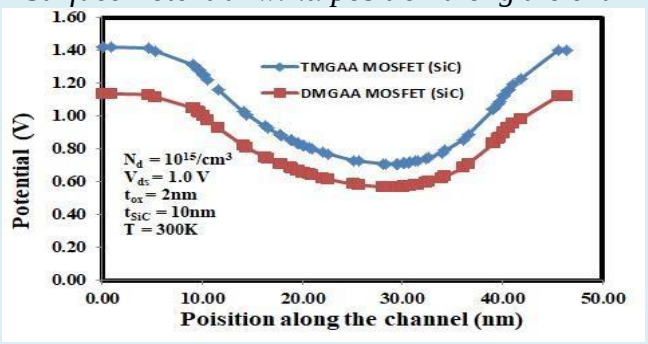
The proposed device employs a TMGAA structure on a 4H-SiC substrate. As shown in Fig. 1(A), the device incorporates three metal gates—Tungsten (Φ = 4.4 eV), Vanadium (Φ = 4.3 eV), and Manganese (Φ = 4.1 eV) each contributing to refined electrostatic control. A cross-sectional view (Fig. 1(B)) illustrates the gate stack, comprising HfO_2 and Al_2O_3, that enhances dielectric properties.Key specifications include a channel length of 25 nm, channel doping of 1×10^{15} cm^{-3}, oxide thickness of 2 nm, and a SiC layer thickness of 10 nm. These parameters are consistent across both DMGAA and TMGAA configurations to ensure fair comparison.

Results And Conclusions:

The TMGAA MOSFET outperforms the DMGAA counterpart in both electrical and analog characteristics due to its advanced gate architecture and optimized material use.

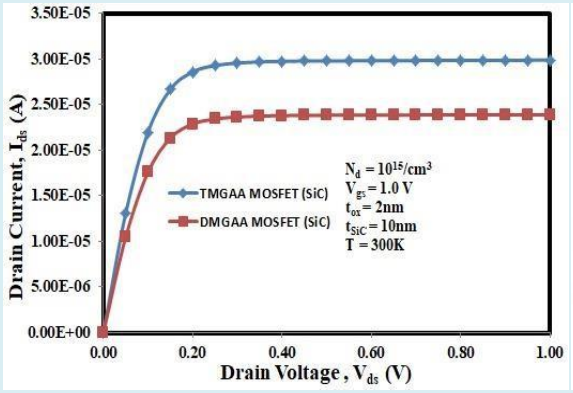
(A) Electrical Characteristics:

Fig. 2 Surface Potential w.r.t. position along the channel for TMGAA MOSFET

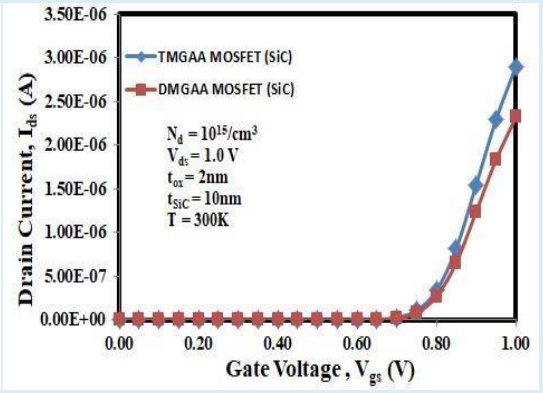


and DMGAA MOSFET (4H- SiC)

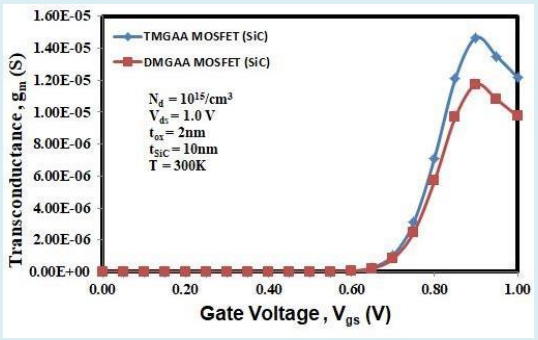
(B) Analog Characteristics:



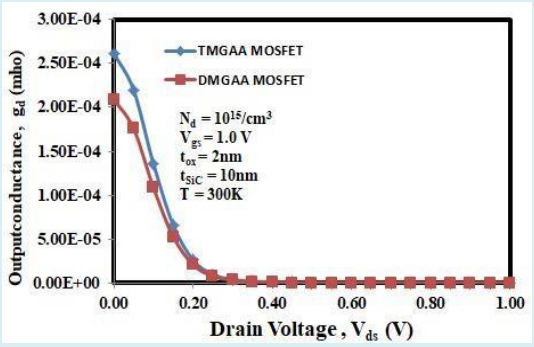
(A)



(B)



(C)



(D)

Fig. 3 (A) Drain Current (I_{ds}) vs. drain voltage (V_{ds}) for DMGAA and TMGAA, (B) Drain Current (I_{ds}) vs. gate voltage (V_{gs}) for DMGAA and TMGAA, (C) Variation Of Transconductance (g_m) vs. gate voltage (V_{gs}) for DMGAA and TMGAA (D) Output Conductance (g_d) vs. drain voltage (V_{ds}) for DMGAA and TMGAA

A. Electrical Characteristics: The TMGAA MOSFET demonstrates a higher peak surface potential (~1.45 V) compared to the DMGAA MOSFET (~1.25 V), reflecting better gate control and reduced short-channel effects. This higher potential profile improves channel modulation, making TMGAA suitable for advanced sensing applications.

B. Analog Characteristics: In terms of analog behavior, TMGAA exhibits superior performance. The drain current (I_{ds}) is higher in both I_{ds}-V_{gs} and I_{ds}-V_{ds} characteristics, attributed to reduced threshold voltage and lower series resistance. The maximum I_{ds} with respect to V_{gs} improves by 29%, and with respect to V_{ds} by 25.63%. The transconductance (g_m) is 27% higher in TMGAA due to efficient gate modulation, and the output conductance (g_d) is also enhanced by 26%. These enhancements collectively lead to reduced short-channel effects and reduces drain induced barrier lowering (DIBL) . These improvements highlight that TMGAA MOSFET provide superior analog performance, making them a better choice for high-frequency and high-power applications compared to DMGAA MOSFETs.

TABLE II RESULT COMPARISON FOR TMGAA MOSFET AND DMGAA MOSFET

Parameters	**DMGAA MOSFET (4H-SiC)**	**TMGAA MOSFET (4H-SiC)**	**% improvement in TMGAA MOSFET with respect to DMGAA MOSFET**
Maximum Drain Current, I_{ds} w.r.t V_{ds}(A)	$2.38x10^{-05}$	$2.99x10^{-05}$	25.63
Maximum Drain Current, I_{ds} w.r.t V_{gs} (A)	$2.32x10^{-06}$	$3x10^{-06}$	29
Peak Transconductance g_m, (S)	$1.17x10^{-05}$	$1.49x10^{-05}$	27
Output Conductance, g_d (mho)	$2.00x10^{-04}$	$2.52x10^{-04}$	26

REFERENCES:

[1] *S.-M. Kang and L. Yusuf, CMOS Digital Integrated Circuits, 3rd ed. New York: McGraw-Hill, 2003.*

[2] *S. Rewari, R. S. Gupta, S. S. Deswal, and V. Nath, ―Silicon carbide based DSG MOSFET for high power, high speed and high frequency application,‖ in Proc. IEEE 6th India Int. Conf. Power Electron. (IICPE), 2015, pp. 1822–1827*

[3] *Neeraj, S. Sharma, A. Goel, and S. Rewari, R. S. Gupta, ―Gate-Stack Dual Metal (DM) Nanowire FET with Enhanced Analog Performance for High Applications,‖ in Proc. DEViC, May 2021, pp. 373–377.*

[4] *C. H. Shih, Y. M. Chen, and C. Lien, ―An analytical model of short channel effect for metal–oxide– semiconductor field-effect transistor with insulated shallow extension,‖ J. Appl. Phys., vol. 43, no. 12, pp. 7993–7996, 2004.*

[5] *Neeraj, S. Sharma, A. Goel, S. Rewari, S. S. Deswal, and R. S. Gupta, ―Impact of Interface Trap Charges on Silicon Carbide (4H-SiC) Based Gate–Stack, Dual Metal, Surrounding Gate, FET (4H-SiC GSDM-SGFET) for Analog and Noise Performance Analysis for 5G/LTE Applications, ‖ ECS J. Solid-State Sci. Technol., vol. 13, 2024.*

[6] *S. Tanaka, ―Theory of the drain leakage current in silicon MOSFETs, ‖ Solid-State Electron., vol. 38, no. 3, pp. 683–691, 1995.*

[7] *A. S. Sedra, Microelectronic Circuits, 7th ed. New York: Oxford Univ. Press.*

[8] *V. M. Srivastava, K. S. Yadav, and G. Singh, ―Drain Current and Noise Model of Cylindrical Surrounding Double Gate MOSFET for RF Switch,‖ in Proc. Int. Conf. Modeling, Optimization Comput. (ICMOC2012), Kumarakoil, Tamil Nadu, Apr. 2012, pp. 517–523*

[9] *Neeraj, A. Goel, S. Sharma, S. Rewari, and R. S. Gupta, ―SiC-based analytical model for gate-stack dual metal nanowire FET with enhanced analog performance, ‖ Int. J. Numer. Model., pp. 0894– 3370, 2022.*

SATELLITE IMAGE PROCESSING

Mr. Rohit Uday Lakhane, Assistant Professor, Department of Electronics and Communication Engineering, Students: Vansh Kalra (02914802821), Prajwal Khandelwal (03014802821), Lakshya Narang (07414802821)

Enormous manpower and numerous resources are thoughtfully applied to foster space technology thus enabling us to launch satellites with a well-defined constellation and having state of the art remote sensing instruments. In order to make the best use of all the hard work put in to this, it is necessary to effectively and efficiently process the data resulting from these instruments on board the satellite. If not, then all efforts shall turn futile. Satellites provide raw images captured far above the earth's surface which should further be processed to take out the meaningful information. Over the years, many attempts have been made to precisely improve the quality of the information that needs to be extracted from the image [1]. An entirely new arena of image processing exclusively for satellite images is under way and better methods and new developments are being reported quite often.

The ever-growing number of satellites in orbit and the newer avenues of remote sensing applications being discovered so often are offering strong motivation to automate the entire process, right from capturing an image, technically called as Image Acquisition, up to the concluding output, as warranted by the particular application. The steps which lead us from capture to conclusion are connected serially which means that the output of a particular step serves as the input for the next step. It therefore follows that an error arising because of a multitude of reasons in any particular step will resonate throughout the serial chain. The corruption thus caused in the final result may well be irreversible, undetectable, and far from the original expected outcome.

The worst case occurs when errors start to creep in at the very first step: Image Acquisition. If that is true, the consequent steps to enhance the image shall remain futile even if state of the art algorithms are implemented. Hence, a detailed understanding of satellite sensor resolution, satellite image pre-processing, satellite image enhancement etc. becomes necessary to achieve an estimate as close as

possible to the expected result. Flawless approach in this regard is crucial for minimizing human intervention due to the enormous amount of data that must be analyzed in real time.

As per a 2011 report from the Ministry of Home Affairs, Government of India, innumerable lives have been lost on account of natural disasters, lakhs of people have been affected and considerable economic damage has been suffered for the period documented between 1980 to 2010 [2]. In June 2013, Kedarnath, situated in the Himalayan state of Uttarakhand, famous for the Kedarnath Temple, was lashed by heavy floods. Media reports blamed lack of coordination between National Disaster Management Authority (NDMA) and Indian Space Research Organisation (ISRO) as many lives were lost although satellite images pointing to this tragedy were readily available [3,4]. Taking a lesson from this incident, when in April 2019, cyclone Fani lashed the cost of Odisha, people were evacuated well in time and all types of losses were minimized. The UN praised Indian Meteorological Department (IMD) for its prompt action in association with ISRO [5]. Satellite images generally have a huge spatial resolution and therefore it is always a great challenge to extract evocative objects from them. This field is broadly categorized under Image Segmentation. In reference [6], the authors have explored this challenge extensively. The aim of their paper is clearly defined which pertains to finding the technique (or algorithm) which provides with optimum threshold value for multilevel thresholding. The purpose of the study is also well elaborated further. The conventional thresholding methods are efficient for bilevel thresholding but they are computationally expensive for multilevel thresholding as they exhaustively search for the optimum values to optimize the objective functions. Hence the authors desire to work upon nature inspired evolutionary algorithms for multilevel thresholding.

Satellites transmit the captured images back to Earth Stations. During transmission, the images often get corrupted with diverse forms of noise. Author in [7] work on the particular problem. Noise can be added to the image during the acquisition process as well due to any kind of fault that may arise in the sensor due to prolonged use and the harsh conditions of deep space. However, the authors have meticulously pointed out that there is more to mere image noise removal. The real purpose is to tackle noise in such a way so that the denoising methods do not introduce blur in the edges and other shortcomings as compared to the actual image. Generally, noise

removal may involve smoothening of the edges which has to be minimized for further processing. A revolutionary technique called as Spectral Imaging has attracted the attention of researchers for its underlying capability to permit extraction of supplementary information which is beyond the competence of the human eye to interpret. A multispectral image captures data within specified wavelengths across the electromagnetic spectrum. Reference [8] deals with this technology. The aim of this research paper is to understand how to minimize the effect of noise in multispectral images, which may arise from phenomenon such as calibration errors, limitations of the capturing device, wear and tear in the operation of sensors during their life cycle, photon effects, and other interfering natural phenomenon. All these issues are quite difficult to control in satellite remote sensing operations. The researchers point out that such imagery involves large spectral redundancy which causes elimination of minor spectral components during the process of noise removal. Owing to this fact, denoising of multispectral images is a challenging task and this underlines the purpose to take up this task and propose a solution to address it. Satellite images are actually a collection of digital numbers arranged in the form of matrix, also known as the pixel values. Image features such as color, wavelength, etc. may be inferred from them. The accuracy of these values is directly linked with the quality of sensors used to capture an image. The dimensions of these pixels and the level of information contained by them lies in the resolution of the sensor. There are basically four types of sensor resolutions as presented in the literature [1], spatial, spectral, radiometric and temporal.

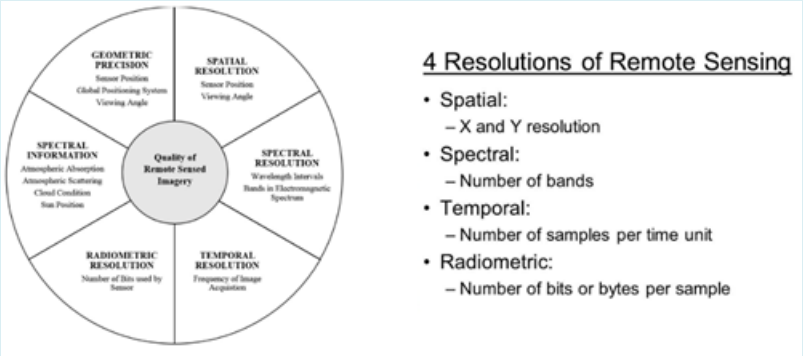


Fig 1. Four types of satellite sensor resolutions [9]

Spatial resolution is the ability to resolve finer details as perceived by the human eye. This parameter is usually expressed in meters. For example, a 30m resolution means that two objects, thirty meters long or wide, sitting side by side, can be separated (resolved) on the captured image. In some specific applications, a

particular wavelength in an image may be of interest. For such cases, spectral resolution is the parameter of choice and it refers to the number of spectral bands (e.g. RGB, NIR, Mid-IR, Thermal, etc.).

A particular range of band may help to extract specific ground features. Panchromatic refers to one band (Black and White), Color 3 bands (RGB), Multispectral 4+ bands (RGBNIR), Hyperspectral (Hundreds of bands). Radiometric resolution is defined as the ability of an imaging system to record many levels of brightness (contrast for example) and to the effective bit-depth of the sensor (number of grayscale levels) and is typically expressed as 8-bit (0–255), 11-bit (0–2047), 12-bit (0–4095) or 16-bit (0–65,535). Temporal resolution means the minimum time required by the satellite to revisit the same location again. This factor is particularly critical for military surveillance. In May 1998, India successfully carried out Nuclear Tests in Pokharan range, Rajasthan. Although the region was under constant surveillance by American spy satellites, the Indian Intelligence carefully dodged them by exploiting the revisit time (temporal resolution) of those satellites over Pokharan area [10].

Once the image has been captured, the next step is the so called Image Preprocessing. Although many preprocessing techniques exist in the literature, there is no standard list for the same. It depends on the application. Selection of a particular technique is critical as preprocessing will alter the original data. Literature survey reveals two main issues for which preprocessing is required: (i) geometric corrections and, (ii) radiometric corrections [1]. Geometric referes to the steps taken to bring an image in synchronization with a map, such as in GPS services or to align the image with other images in order to make a large image from a set of images. Radiometric refers to the adjustment of digital numbers as, described above, in order to account for atmospheric conditions such as cloud cover or a hazy atmosphere.

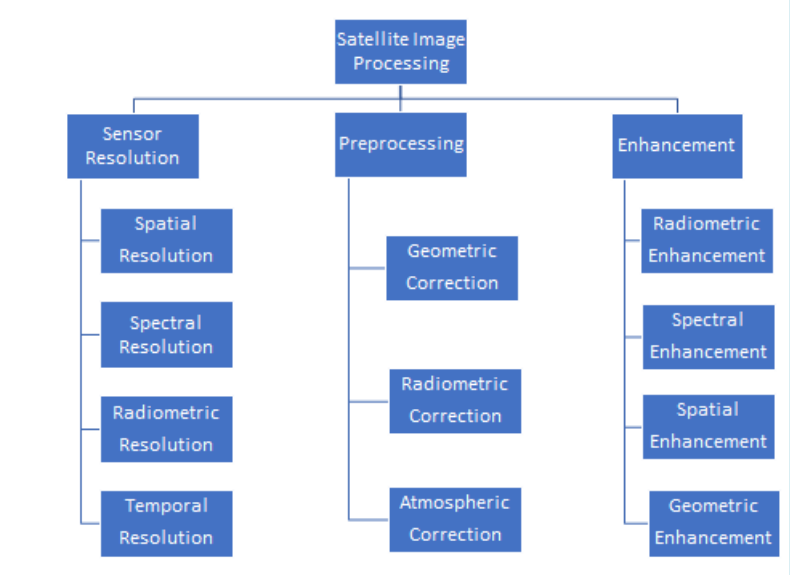


Fig 2. Various Satellite Image Processing techniques as discussed in this section of the report.

Preprocessing is also called as Image Rectification or Image Restoration in the literature. To conclude, this step helps to address degraded/distorted data so as to create a better representation of the original image. Preprocessed image should remain faithful to its original counterpart. Once preprocessing is done, image enhancement techniques are applied for superior visual elucidation of the image. In the literature, enhancement techniques have been categorized broadly under four types: Radiometric, Spectral, Spatial and Geometric. In order to analyze a particular feature(s) of Earth's surface, Radiometric Enhancement is used. It basically improves the contrast between pixels lying in some predefined range by assigning it specific screen colors. Spectral Enhancement is expended to generate new spectral data from available bands. This is achieved by modifying pixel values by using some operation based upon pixel-by-pixel basis. Spatial Enhancement works on pixels directly based upon the neighborhood pixels. Examples of spatial enhancement include image sharpening, image smoothening and other such operations. Lastly, Geometric Enhancement is performed for edge detection, line detection, etc. which generally leads to image sharpening. This type of enhancement is significant for applications such as road mapping, urban planning, etc. where edge and line detection is heavily required.

Image Transformation techniques are employed for multitemporal imaging data, i.e., images of the same location taken at different times. Since the times are different,

the set of images of the same location may differ in the sense that capturing conditions may vary considerably. For example, atmospheric noise, angle of satellite sensor, seasonal changes, day/night illumination on the area, etc. will vary. Transformation involves basic arithmetic operations. To combat noise, addition operation is performed on the set of images. Subtraction is used to detect changes in the images that have taken place over time. Multiplication operation gives the basis to extract region of interest while division is used for ecological and agricultural applications.

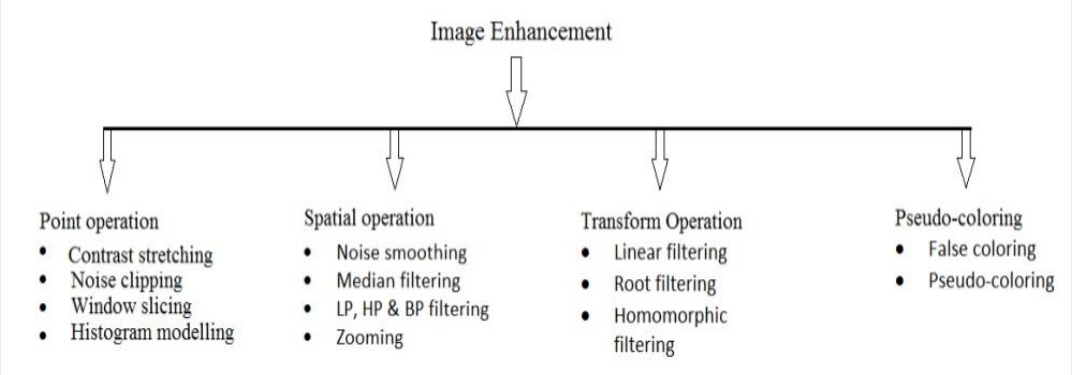


Fig 3. Some Image Enhancement Techniques [11]

Remote Sensing is a technique employed to gather data about an object of interest without having any physical contact with it whatsoever. It has profound application in managing as well as understanding the way mankind is using the natural resources available on Earth, which are already under stress owing to a multitude of reasons ranging from issues like global warming, climate change, pollution, rising sea levels etc. and further escalated due to human greed, political causes and the desire of nations to have maximum control of natural resources under their possession. In technical terms, these natural resources can be classified into various categories such as forest area, vegetation, agriculture, water body, barren land etc. Once this classification is determined, any satellite image of some geographical region, captured for that purpose, may be converted into a "thematic map" for that particular region which is visually enhanced so as to clearly depict all the chosen categories of interest as per the classification. The word "thematic" is derived from the English word "theme", meaning, "some common aspect in a broad subject matter". Development of such a map from remotely sensed satellite imagery is termed as Image Classification. Other than mapping natural resources, it is also beneficial in several other applications such as urban planning, natural disaster management,

studying the effects of global warming, military supervision of suspected activity in a remote area and so on.

In the literature, Image Classification methods have been broadly categorized into three categories: Automated, Manual and Hybrid [12]. Classified maps have a wide range of applications and in order to get reliable analysis offered by them, it is necessary that we have some idea of accuracy of the classified map. Therefore, there must be carefully planned accuracy assessment tests and the source of accuracy should also be known. Classified map is basically an approximate representation of the features on the ground. Accuracy of this representation will further affect the quantitative analysis done using them as in case of landscape metrics calculation.

CONCLUSION

The work done till date in the field of satellite image processing has been estimated in this technical article. Overall, twenty four research papers were studied and apart from these twenty four papers, a few more papers were also read. Following inferences can be drawn from this technical article:

- Computational Complexity is a major issue in satellite image processing. For real time processing, it must be as low as possible.
- Due to high spatial resolution of remotely sensed images, image segmentation remains a challenging task. Nature inspired algorithms are being used to solve this problem.
- Noise due to internal and external sources often corrupt the image. Moreover, errors are prone during the transmission to Earth station as well. Research is being directed toward minimising the effects of noise and distortion over original image pixels.
- Image Fusion is a way to combine several images taken over different times of the same geographical area, or, taken by various satellites at different viewing angles. It involves geometric corrections so that a combined image may be produced.
- Image Fusion is also used to combine multispectral and hyperspectral images.
- Application of remote sensing in areas such as land cover classification requires accurate Image Classification techniques that assign the pixel to its

correct class. Incorrect classification results in errors in land metric calculations that is obtained from the thematic maps thus generated.

- For hyperspectral images, at some wavelengths, atmospheric effect between the target and the sensor may be quite considerable thus requiring atmospheric correction prior to further processing. This is necessary for a solution to estimate atmospheric parameters such as temperature and water vapor content from HS images.
- Multispectral image denoising is relevant as noisy images not only affect human interpretation but also limit the effectiveness of other image enhancement techniques that may be employed as those techniques might enhance the noise in same proportions. It also renders software analysis data to be less reliable. Therefore, proper denoising methods have to be developed as a prerequisite.

REFERENCES

[1] J. B. Campbell, "Introduction to Remote Sensing," 3rd Edition, The Guilford Press, New York, 2002.

[2] "Table 1.4: People affected, lives lost and economic damage due to Disasters in India between 1980 to 2010", https://www.undp.org/content/dam/india/docs/disaster_management_in_india.pdf, Ministry of Home Affairs, Government of India.

[3] NDMA says ISRO gave no warning to Uttarakhand, https://www.indiatoday.in/india/north/story/ndma-passes-the-buck-says-no-prior-warning-was-given-by-isro-on-uttarakhand-168910-2013-07-02

[4] SCATSAT-1 – Satellite for Weather Forecasting, Cyclone Detection and Tracking, Department of Space, Indian Space Research Organisation, https://www.isro.gov.in/scatsat-1-–-satellite-weather-forecasting-cyclone-detection-and-tracking

[5] UN Praises Met Dept for 'Pinpoint Accuracy' on Cyclone Fani That Minimised Loss of Life, https://www.news18.com/news/india/un-praises-met-dept-for-pinpoint-accuracy-on-cyclone-fani-that-minimised-loss-of-life-2127883.html

[6] A.K. Bhandari, V.K. Singh, Anil Kumar and G.K. Singh, "Cuckoo search algorithm and wind driven optimization based study of satellite image segmentation

for multilevel thresholding using Kapur's entropy", Expert Systems with Applications, Volume 41, Issue 7, 1 June 2014, Pages 3538-3560.

[7] A.K. Bhandari, D. Kumar, A. Kumar and G.K. Singh, "Optimal sub-band adaptive thresholding-based edge preserved satellite image denoising using adaptive differential evolution algorithm",Neurocomputing, Volume 174, Part B, 22 January 2016, Pages 698-721.

[8] S. Suresh, S. Lal, C. Chen and T. Celik, "Multispectral Satellite Image Denoising via Adaptive Cuckoo Search-Based Wiener Filter", IEEE TRANSACTIONS on Geoscience and Remote Sensing, Vol. 56, Issue 8, Aug. 2018.

[9] The Ohio State University, College of Food, Agricultural and Environmental Sciences, https://ohioline.osu.edu/factsheet/fabe-5541

[10] "NUCLEAR ANXIETY: THE BLUNDERS; U.S. Blundered On Intelligence, Officials Admit", By Tim Weiner, May 13, 1998, The New York Times.

[11] Presentation on Image Enhancement at National Aerospace Laboratories, A.R. Kambi, Samatha H S, Sanjana G S, Surabhi K S under guidance of Mr. Lokesha H, Senior Scientist, DSPS group, ALD division, NAL.

[12] Horning, N. 2004. "Land cover classification methods", Version 1.0. American Museum of Natural History, Center for Biodiversity and Conservation. Content is available at the link http://biodiversityinformatics.amnh.org.

Next-Gen Gas Detection: A Junctionless Nanowire Ferroelectric FET for PH_3 Sensing

Ms. Shalu Garg, Assistant Professor, Department of Electronics and Communication Engineering, Student: Anurag Rungta (21114802822), Sandhya Tiwari (21514802822)

Abstract

The detection of phosphine (PH_3)—a hazardous yet industrially relevant gas—has been tackled through the development of a cutting-edge device: the **Junctionless Nanowire Ferroelectric Field Effect Transistor (J-NW-Fe-FET)**. Designed with high-k materials and negative capacitance physics, this device achieves exceptional sensitivity at room temperature using catalytic gate materials (Cr, Ir, Rh). The simulation-driven study offers insights into its operational mechanisms and performance enhancements.

Background and Need

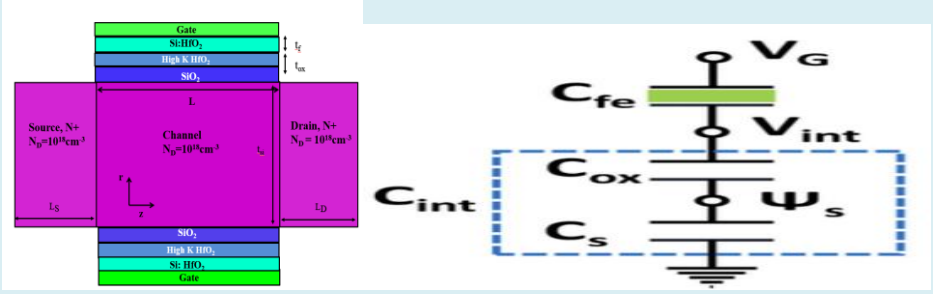
Phosphine gas, though widely used in agriculture and semiconductors, poses a significant health hazard. Detecting trace amounts with low-power, sensitive devices has been a challenge—especially at room temperature. Field-effect transistors (FETs), particularly those with nanowire architectures, offer high surface-area-to-volume ratios and strong gate control, making them excellent candidates for gas sensing.

Device Overview

The **J-NW-Fe-FET** architecture introduces three major innovations:

1. **Junctionless Design** – Reduces leakage and simplifies fabrication.
2. **Ferroelectric HfO_2 Layer** – Enables subthreshold swing below 60 mV/decade via negative capacitance.
3. **Catalytic Metal Gates** – Chromium (Cr), Iridium (Ir), and Rhodium (Rh) facilitate gas interaction, altering work functions and triggering electrical changes.

Simulation was carried out using the **ATLAS 3D simulator**, incorporating models for mobility, quantum effects, and ferroelectric behavior.



Sensing Mechanism

When PH_3 molecules interact with the metal gate:

- **Phosphorus**, an n-type dopant, donates electrons.
- This **lowers the gate's work function**, shifting the Fermi level.
- The shift impacts **threshold voltage**, **drain current**, and overall transistor characteristics.

Iridium showed the most substantial response, improving surface potential and carrier concentration significantly. The strong catalytic activity of Ir also promoted better transconductance and output conductance.

Key Findings

- **Electron Concentration**: Iridium demonstrated the highest increase after PH_3 exposure.
- **Drain Current**: Chromium initially had higher current due to a lower work function, but Iridium surpassed it post-PH_3 diffusion due to effective charge transfer.
- **Transconductance & Output Conductance:** Ir outperformed Cr and Rh, especially for shorter channel lengths (30 nm).
- **Scalability**: Reduced channel lengths increased the current due to negative capacitance-induced voltage boosting.

Conclusion

The proposed J-NW-Fe-FET offers a **power-efficient, room-temperature operable, and scalable platform for phosphine gas detection**. Among the catalytic metals tested, **Iridium emerged as the most effective**, balancing sensitivity and stability. Incorporating ferroelectric layers adds another level of performance optimization, making the device suitable for integration into modern IoT-based environmental or industrial monitoring systems.

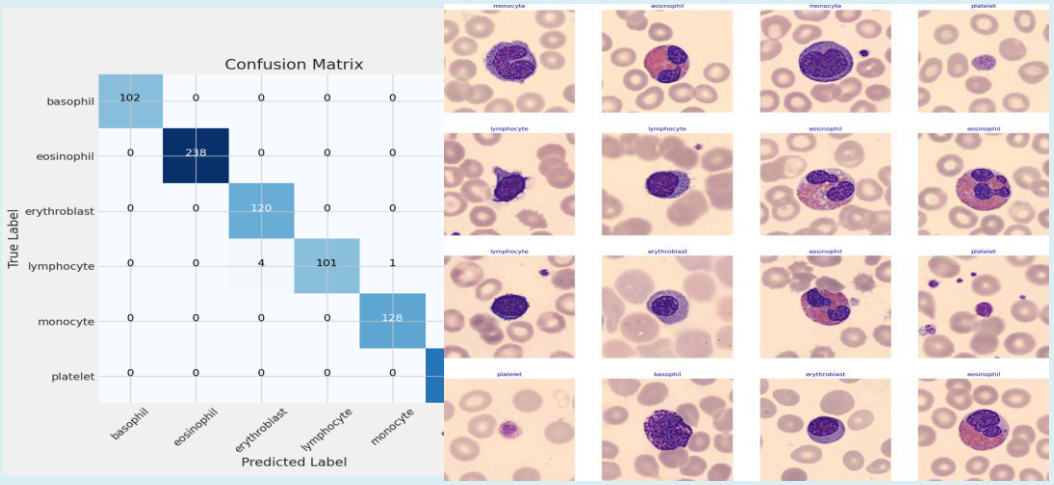
Blood Cancer & Leukemia Identification Using Hybrid Ensemble Deep Learning

Prof. (Dr.) Sunil Kumar, HOD, Department of Electronics and Communication Engineering, Students: Raghav Gupta, Akshat Bhardwaj, Varun Sharma

Blood cancers including leukemia, lymphoma, and myeloma—are among the most complex and deadly forms of cancer, largely due to their subtle onset, overlapping symptoms, and the difficulty of early-stage detection. Traditional diagnostic methods, such as blood tests, biopsies, and genetic analyses, though essential, can be invasive, time-consuming, and reliant on expert interpretation. In recent years, advances in artificial intelligence, particularly deep learning, have paved the way for innovative approaches to disease diagnosis. This article explores the implementation of a **hybrid ensemble deep learning model** designed to improve the detection and classification of blood cancers using multi-modal clinical and genomic data.

At the core of this hybrid model lies the integration of two powerful convolutional neural network (CNN) architectures: **Residual Networks (ResNet)** and **Visual Geometry Group networks (VGG)**. ResNet is known for its use of identity shortcuts to tackle the vanishing gradient problem, allowing for deeper networks capable of learning complex patterns in medical images. On the other hand, VGG networks offer simplicity and depth, excelling at extracting fine-grained features from cellular images. By combining these models in an ensemble framework, the system leverages their individual strengths to improve diagnostic performance.

The study utilized a comprehensive dataset composed of blood smear images, bone marrow biopsy slides, gene expression profiles, and clinical records. After preprocessing steps such as image normalization, data augmentation, and feature selection from genomic data, the ResNet and VGG models were trained separately and later combined through ensemble techniques like **bagging and boosting**. These ensemble strategies allow for greater robustness and reduced model bias, which is critical in medical contexts where even small errors can have significant consequences.



The results of this hybrid approach were compelling. The ensemble model achieved a **diagnostic accuracy of 94.8%**, significantly outperforming the individual ResNet (87.3%) and VGG (89.2%) models. Notably, it also demonstrated superior precision (93.4%), recall (96.1%), and F1-score (96.2%), underscoring its capability to correctly identify true positive cases of blood cancer. The high recall rate is particularly important for clinical use, as missing a positive case can have life-threatening implications.

In addition to superior performance, this model supports early diagnosis and potentially **personalized treatment strategies** by identifying disease markers from both visual and genomic data. This integrated diagnostic view is essential in modern oncology, where therapies are increasingly tailored to a patient's unique genetic profile.

However, the hybrid model is not without its challenges. Data quality and diversity remain key hurdles. Many medical datasets are either small or imbalanced, limiting the generalizability of AI models across varied populations. Moreover, the interpretability of deep learning systems is a critical concern in healthcare; physicians must be able to trust and understand AI-generated decisions. As such, further research into **explainable AI** and **interpretable models** will be necessary to ensure the successful integration of such tools into clinical workflows.

In conclusion, the hybrid ensemble deep learning model marks a significant step forward in the diagnosis of hematological cancers. By combining deep neural networks with ensemble

learning strategies, this approach not only improves diagnostic accuracy but also offers a scalable, less-invasive solution that could revolutionize early detection efforts. With ongoing improvements in data collection, computational power, and AI interpretability, such hybrid systems have the potential to become integral components of future clinical oncology, enhancing outcomes and guiding more effective treatments for patients worldwide.