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MAHARAJA AGRASEN INSTITUTE OF TECHNOLOGY

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DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

TECHVOLVE

(2022-23)

(TECHNICAL MAGAZINE)

UNVEILING THE POWER OF CIRCUITS AND WAVES

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Maharaja Agrasen Institute of Technology

(Department of Electronics and Communication Engineering)

VISION

To excel in technical education and provide a valuable resource to Electronics Industry and Society.

MISSION

To develop a strong Centre of Excellence for technical education enabling students to be competent professionals with respect to Electronics Industry having entrepreneurial skills who are also responsible citizens with ethical and social values.

M1: Promote Effective Teaching - learning process in the field of Electronics and Communication to provide in-depth knowledge to the students of the curriculum, beyond curriculum and interdisciplinary aspects.

M2: Develop a strong Centre of Excellence for technical education and research attracting the best intellectuals from Academics & Industry and also encouraging the students to pursue higher studies in the field of Electronics & Communication.

M3: Inculcate creative thinking among students which enhances their entrepreneur skills, employability and research capabilities.

M4: Enable students to be competent professionals with Industrial aptitude ready to face the challenges due to globalization.

M5: To create social, ethical, cultural and human values in students so that they are responsible citizens of the society.

Maharaja Agrasen Institute of Technology

(Department of Electronics and Communication Engineering)

PROGRAM EDUCATIONAL OBJECTIVES (PEOs)

PEO1. To ensure that the Electronic & Communications graduates have the core competency to be successful in Industry/Technical profession or to excel in post-graduate programs and research activities

PEO2. To inculcate in graduates an ability to analyze real life problems and design appropriate system to provide solutions that are technically sound, economically feasible and socially acceptable.

PEO3. To inculcate in students professionalism, effective communication skills, teamwork, multidisciplinary approach and an ability to relate Electronics engineering issues to broader contexts.

PEO4. Provide an environment that gives adequate opportunity to the students to cultivate lifelong skills and develop leadership qualities needed for a successful professional career.

PEO5. To develop social, ethical & human values in students so that they become responsible citizens & contribute towards social wellbeing of the society.

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PROGRAM SPECIFIC OUTCOMES (PSOs)

PSO1: Professional skills: An ability to understand the basic concepts in Electronics & Communication Engineering and to apply them to various areas, like Semiconductors, Communications, Signal Processing, Antenna, Networking, VLSI, Computing, Embedded systems and to be mastered the latest tools and techniques used in the field of research and industry.

PSO2: Problem solving skills: An ability to face various problems in the area Electronics and Communication Engineering using latest hardware and software tools.

PSO3: Successful Career: An understanding of social-awareness & environmental-wisdom along with ethical responsibility to have a successful career and to sustain passion and zeal for real-world applications using optimal resources as an Entrepreneur.

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Message from the Head of the Department

It is a matter of great pride and joy to present the latest edition of TECHVOLVE, the annual technical magazine of the Department of Electronics and Communication Engineering. This publication is not just a compilation of articles it is a reflection of the enthusiasm, creativity, and relentless curiosity that define our department's culture.

Over the past year, our students and faculty have continued to explore the rapidly evolving domains of nanotechnology, VLSI design, embedded systems, communication networks, artificial intelligence, and the Internet of Things. These advancements are shaping the future of technology and transforming the way we live, work, and communicate. Through TECHVOLVE, we aim to capture this spirit of innovation, providing a platform for sharing knowledge, research insights, project outcomes, and thought-provoking ideas.

I am pleased to see that our students have risen to the challenge, engaging in research projects, hackathons, paper presentations, industrial training, and

community outreach initiatives. The diversity of contributions in this edition demonstrates their ability to blend academic knowledge with real-world application, a skill that will serve them well in their professional journey.

My best wishes to the entire ECE fraternity for continued success, and may this magazine continue to serve as a beacon of knowledge and inspiration for years to come.

Dr. Sunil Kumar
Head of Department, ECE

Maharaja Agrasen Institute of Technology

(Department of Electronics and Communication Engineering)

Table of Content

Design of First Order Active Low Pass Filter using 22nm Gate All Around Silicon-on-Insulator Schottky Barrier MOSFET

Mr. Amit Saxena, Assistant Professor, Department of Electronics and Communication Engineering, Students: Ms. Shruti Jain(02514802819), Ms. Arshia Vashisht(35514802819) and Mr. Joyesh Banerjee(14014802819)

Abstract: The analog/RF parameter analysis is performed for 22nm gate all around silicon-on-insulator schottky barrier (SOISB) MOSFET for circuit applications. The small-signal model parameters are extracted for SOISB MOSFET. A first-order active low pass filter using three SOISB MOSFETs is proposed in this work. NMOS SOISB MOSFET is used as a resistor with a grounded capacitor for performing filtering action. For amplification of filtered signal CMOS SOISB MOSFET amplifier is used in the output stage. Further gain and phase analysis of the low pass filter circuit is performed with cut-off frequency.

Index Terms: SOISB MOSFET, schottky barrier, low pass filter, MOSFFT-C.

I. INTRODUCTION

The high-density integration and low power consumption circuit's demands in the semiconductor industry, results scale down the size of MOSFET. The aggressive reduction in the channel length of MOSFET leads to several types of problems due to short channel effects (SCE's)[1-4]. To minimize the unwanted effects of SCE's, many new MOSFET architectures are under investigation. Recently gate all around silicon-on-insulator schottky barrier (SOISB) MOSFET is proposed for high transconductance (gm), low power consumption, and high linearity parameters [5-6].

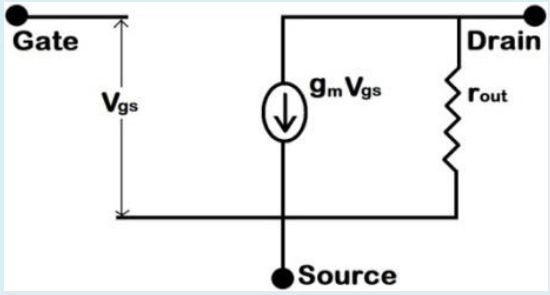

Fig.1 Simplified small-signal model for SOISB MOSFET for saturation region only.

In this work, the simplified small-signal model for SOISB MOSFET is extracted with the minimum parameter for analog circuit applications. Fig1. shows the small-signal model assuming that MOSFET is in the saturation region only. The model is extracted with only two parameters transconductance (gm) and output resistance (rout). Further first order low pass MOSFET-C filter is designed by using SOISB NMOSFET as active load in place of passive resistance for 1mv input signal. The low pass filter is designed for 1nF, 0.01nF, and 1pF capacitor values. To obtaining an amplified output signal CMOS-SOISB amplifier is used in the output stage. The voltage gain and overall phase change of the active low pass filter with frequency are analyzed.

II. DEVICE STRUCTURE

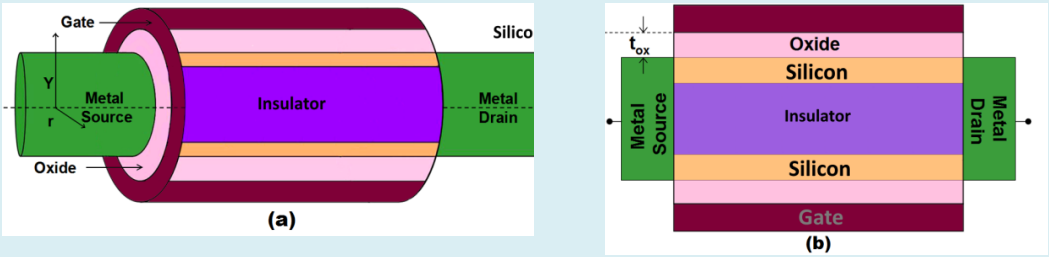

Fig.2 (a) Gate all around SOISB NMOSFET with three dimensional view and (b) with two dimensional view.

TABLE I

STRUCTURE DEVICE PARAMETERS USED FOR NUMERICAL SIMULATION

Parameter	SOI SB
Length of channel (nm)	22
Doping of channel (cm^{-3})	10^{15}
Thickness of gate oxide (nm)	2
Diameter of silicon pillar (nm)	10
Metal work-function (eV)	4.8
Dielectric length (nm)	22
Radius of dielectric (nm)	2

The three-dimensional and two-dimensional device structural views of the gate all around SOISB NMOSFET are presented in Fig 2. (a) and (b) respectively. The device parameters channel length, n-type doping, SiO2 gate oxide thickness, SiO2 insulator dielectric pillar thickness, metalwork function used for device simulation are defined in Table I. The atlas silvaco TCAD is used for numerical device simulations.

III. ANALOG DEVICE PARAMETERS

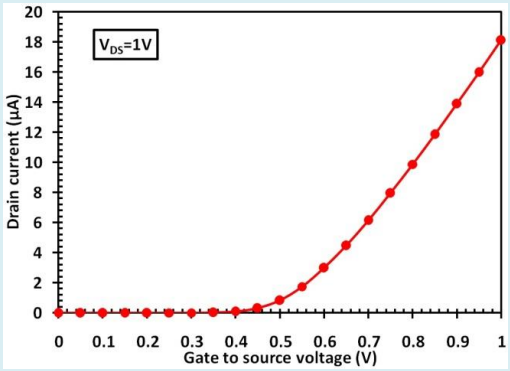

Fig.3 The plot of drain current vs. gate to source voltage for gate to all SOISB NMOSFET.

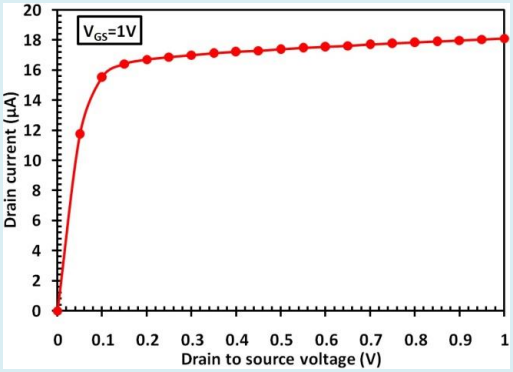

Fig.4 The plot of drain current vs. drain to source voltage for gate to all SOISB NMOSFET.

The plot of the gate all around SOISB NMOSFET drain current (ID) vs. gate to source voltage (VGS) at the constant drain to source voltage (VDS) at 1V is plotted in Fig.3. The numerically calculated value of threshold voltage (Vt0) for gate all around SOISB NMOSFET is 0.428V. The maximum value of drain current (ID) at VGS=1V and VDS=1V is nearly 18μA. Fig. 4 shows the plot of drain current (ID) vs. gate to source voltage (VGS) at the constant drain to source voltage (VDS) =1V for gate all around SOISB NMOSFET. The maximum value of drain current (ID) in the saturation region at VDS=1V and VGS=1V is nearly 18 μA. For the design of a low pass filter, the gate all around SOISB NMOSFET is used as active load by applying a gate biased of 0.25V. As shown in Fig 1. The small-signal model used contains only two device parameters, transconductance (gm) and output resistance (rout).

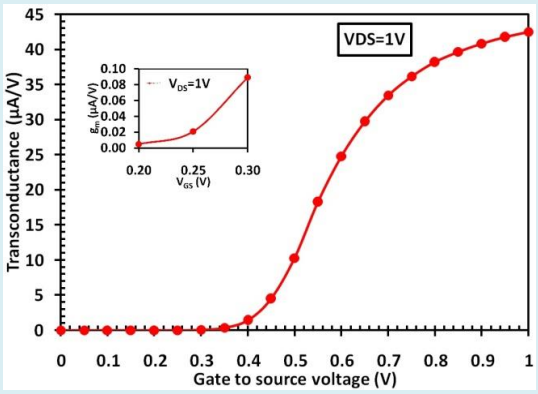

Fig.5 The transconductance (gm) plot vs. gate to source voltage for gate all around SOISB NMOSFET.

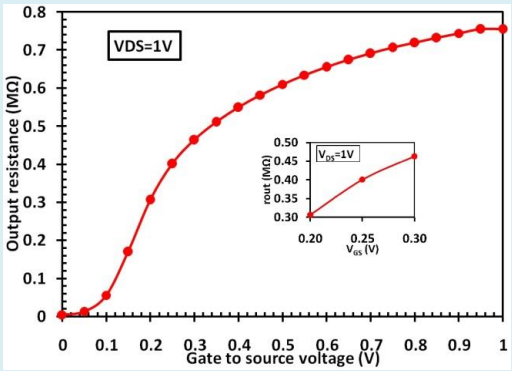

Fig.6 The output resistance (rout) plot vs. gate to source voltage for gate all around SOISB NMOSFET.

Fig. 5 and Fig. 6 show the plots of transconductance (gm) and output resistance (rout) of the gate all around SOISB NMOSFET vs. gate to source voltage (VGS) at the constant drain to source voltage (VDS)=1V respectively. The values of transconductance (gm) and output resistance (rout) for 0.25V of gate bias are 0.0207μS and 0.4008 MΩ respectively.

IV. CMOS SOISB VOLTAGE AMPLIFIER

The proposed first-order active low pass filter is designed for a 1mV input signal. So, it is required to increase the voltage amplitude of the output signal. For the amplification of the processed input signal, a gate all around SOISB CMOS voltage amplifier circuit is used at the output stage.

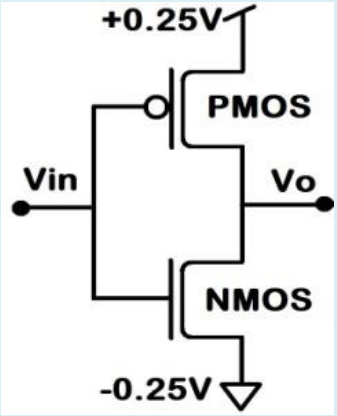

Fig.7 Gate all around SOISB CMOS voltage amplifier circuit.

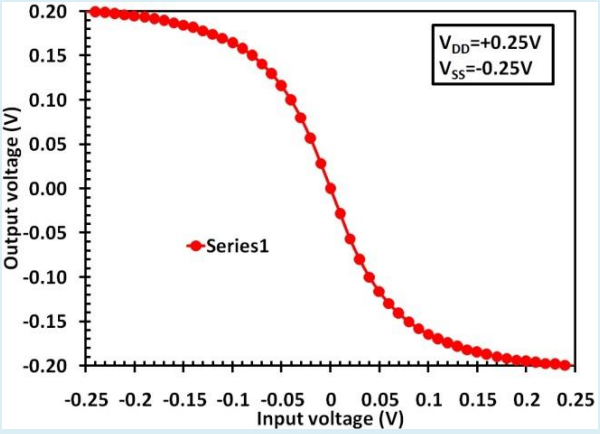

Fig.8 Voltage transfer characteristics for gate all around SOISB CMOS voltage amplifier circuit.

The circuit diagram of the gate all around the SOISB CMOS voltage amplifier is shown in Fig. 7. The voltage amplifier circuit uses 22nm SOISB PMOSFET and

NMOSFET. The circuit is driven by a positive power supply VDD of +0.25V and a negative power supply VSS of -0.25V. Fig. 8 shows the voltage transfer characteristics of the CMOS SOISB voltage amplifier circuit.

V. ACTIVE LOW PASS FILTER CIRCUIT

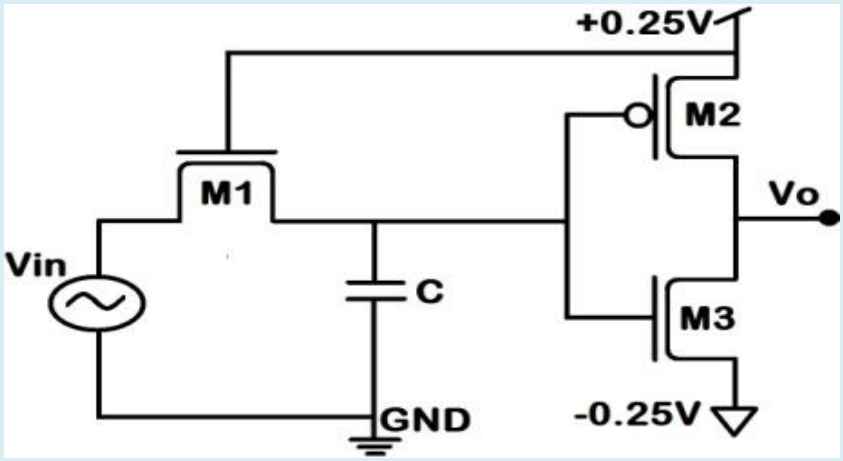

Fig.9 Circuit diagram of first order active low pass filter.

The circuit diagram of first-order active low pass filter using gate all around SOISB MOSFET is shown in Fig. 9. The M1 SOISB NMOSFET is gate biased with +0.25V and works as an active load. Using the small-signal model shown in Fig.1, the equivalent active resistance (Req) of M1 SOISB NMOSFET can mathematically be expressed as:

$$R_{eq} = \frac{\left(1/g_{m1}\right)\times r_{out1}}{\left(1/g_{m1}\right)+r_{out1}} \qquad (1)$$

The values of gm1 and rout1 for M1 MOSFET are 0.0207µS and 0.4008 MΩ respectively at +0.25V gate bias. The calculated numerical value of Req is 397.5KΩ. The M2 & M3 are SOISB PMOSFET and NMOSFET respectively; they form a CMOS voltage amplifier with a voltage gain of Av. The mathematical expression of transfer function H(s), phase (φ), and cut-off frequency (Fc) for first-order active low pass filter shown in Fig.10 is given by:

$$H(s) = \left[\frac{A_v}{s+\left(\frac{1}{R_{eq}\times C}\right)}\right] \qquad (2)$$

$$\varphi = -tan^{-1}\left(2\pi f R_{eq} C\right) \qquad (3)$$

$$F_c = \left(\frac{1}{2\pi R_{eq} C}\right) \quad (4)$$

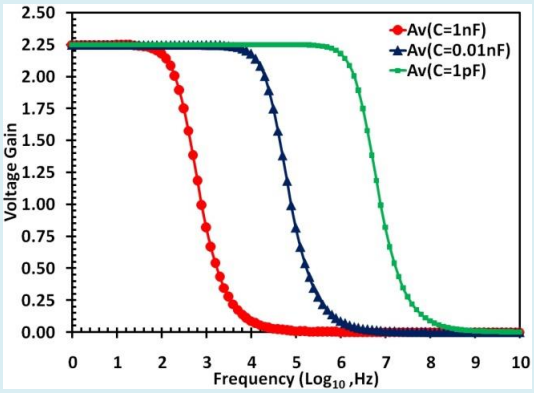

Fig.10 Plot of transfer function H(s) vs. input signal frequency in linear scale for 1nF, 0.01nF and 1pF capacitor values.

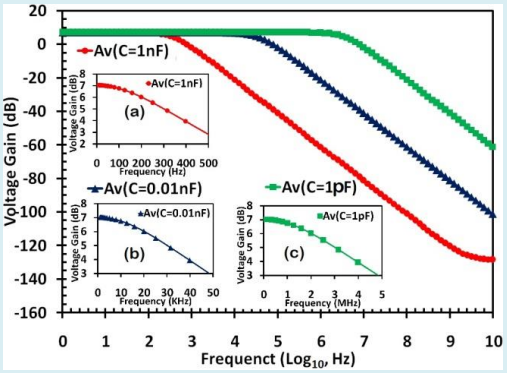

Fig.11 Plot of transfer function H(s) vs. input signal frequency in log scale for 1nF, 0.01nF and 1pF capacitor values.

An ac input signal of 10mV is applied at the input of the low pass filter circuit shown in Fig.9. The plot of the transfer function H(s) of low pass filter vs. frequency of input signal is shown in Fig.10. The transfer function H(s) is plotted for three different values of the capacitors (C) 1nF, 0.01nF, and 1pF respectively in a linear scale.

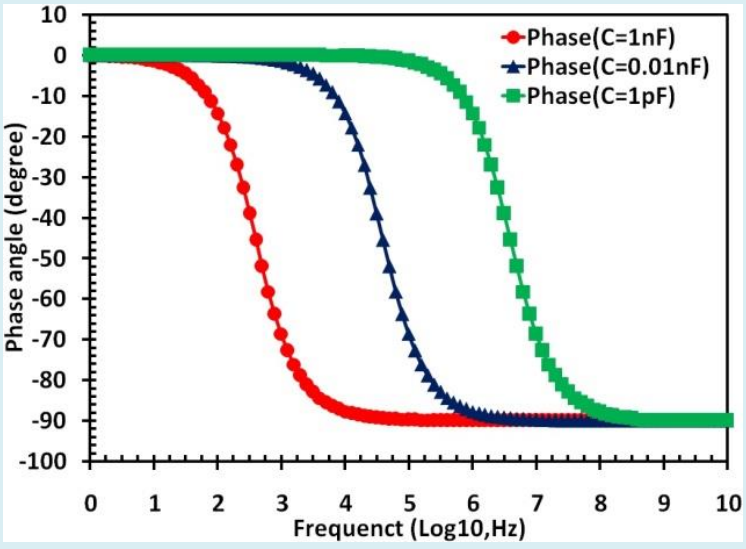

Fig.12 Plot of phase (φ) vs. input signal frequency for 1nF, 0.01nF and 1pF capacitor values.

Fig .11 shows the plot of the transfer function H(s) in dB vs. input signal frequency. The cut-off frequencies for 1nF, 0.01nF, and 1pF capacitor values are 400.5928 Hz, 40.0592 kHz, and 4.0059 MHz respectively. The plot of change in phase angle (φ)

with input signal frequency is shown in Fig. 12 for capacitor (C) values of 1nF, 0.01nF, and 1pF respectively.

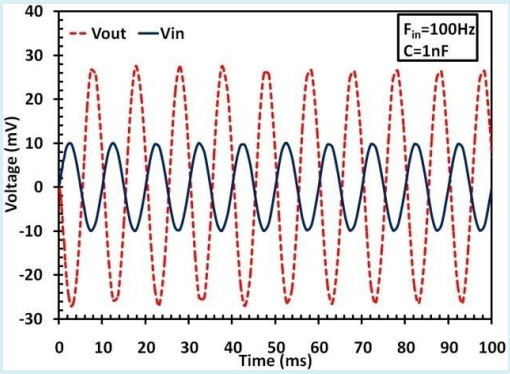

Fig.13 Transient response of active low pass filter for 1mV and 100Hz input signal.

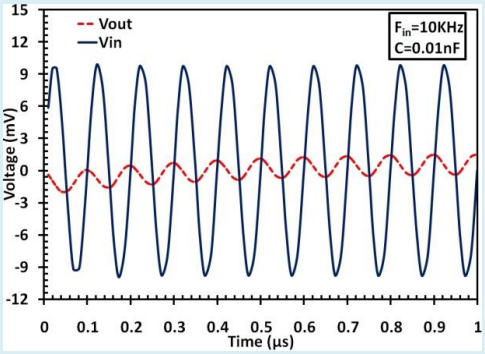

Fig.14 Transient response of active low pass filter for 1mV and 10KHz input signal.

Since the active low pass filter must amplify all input signals with frequency less than cut-off frequency and attenuates all input signals having frequencies greater than cut-off frequency. For C=1nF the cut-off frequency (fc) of the low pass circuit is 400.5928 Hz. The transient analysis of active first order low pass filter circuit for 10mV 100 Hz and 10 kHz ac input signal with C=1nF are shown in Fig.13 and Fig. 14 respectively.

An ac input signal of 10mV and 100Hz frequency is applied as input to the low pass filter circuit. Since the ac input signal frequency is less than the cut-off frequency the output voltage (Vo) is amplified and equals 27.1483 mV as shown in Fig. 13. But for an ac input signal of 10 mV and 10 kHz, the output signal is attenuated as shown in Fig. 14.

VI. CONCLUSION

The simplified small-signal model parameters as shown in Fig. 1 are extracted for 22nm gate all around SOISB MOSFET. The active first order low pass filter using gate all around SOISB MOSFET's is designed. The transfer function H(s), phase (φ), and cut-off frequency (fc) are calculated and using the extracted simplified small-signal model. The TCAD simulation shows the same results for transfer function H(s), phase (φ), and cut-off frequency (fc).

References

[1] *S. Cristoloveanu and G. Ghibaudo, "Intrinsic Mechanism of Mobility Collapse in Short MOSFETs," in IEEE Transactions on Electron Devices, vol. 68, no. 10, pp. 5090-5094, Oct. 2021, doi: 10.1109/TED.2021.3105083.*

[2] *Y. Jing, J. Zhou and P. Zhou, "Parasitic Capacitance Modeling of Si-Bulk FinFET-Based pMOS," in IEEE Transactions on Electron Devices, vol. 68, no. 10, pp. 4819-4825, Oct. 2021, doi: 10.1109/TED.2021.3101791.*

[3] *G. Pahwa, P. Kushwaha, A. Dasgupta, S. Salahuddin and C. Hu, "Compact Modeling of Temperature Effects in FDSOI and FinFET Devices Down to Cryogenic Temperatures," in IEEE Transactions on Electron Devices, vol. 68, no. 9, pp. 4223-4230, Sept. 2021, doi: 10.1109/TED.2021.3097971.*

[4] *J. Pruefer et al., "Compact Modeling of Nonlinear Contact Effects in Short-Channel Coplanar and Staggered Organic Thin-Film Transistors," in IEEE Transactions on Electron Devices, vol. 68, no. 8, pp. 3843-3850, Aug. 2021, doi: 10.1109/TED.2021.3088770.*

[5] *Saxena, R. K. Sharma, M. Kumar and R. S. Gupta, "Linearity Investigation of Ultra-Low-Power Cylindrical SOI Schottky Barrier MOSFET for Biomedical and 5G/LTE Circuits Application," 2021 Devices for Integrated Circuit (DevIC), 2021, pp. 363-367, doi: 10.1109/DevIC50843.2021.9455863.*

[6] *"SOI Schottky Barrier Nanowire MOSFET with Reduced Ambipolarity and Enhanced Electrostatic Integrity."Journal of Electronic Materials, Springers. Journal of Elec Materi 49, 4450–4456 (2020). https://doi.org/10.1007/s11664-020-08164-0.*

Applications of Machine Learning in Wireless Communication Systems

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Abstract: The rapid evolution of wireless communication networks, from 2G to 6G, has introduced unprecedented complexities in managing resources, mitigating interference, and improving network performance. Traditional rule-based optimization methods are increasingly inadequate to meet the dynamic requirements of modern networks. Machine Learning (ML), with its capability to learn patterns from data and adapt to environmental changes, has emerged as a powerful tool to enhance wireless communication systems. This paper explores the key applications of ML in wireless communication, including signal detection, channel estimation, spectrum management, beamforming, and resource allocation. It also highlights existing challenges and future research directions for integrating ML into wireless systems.

Keywords: Machine Learning, Wireless Communication, Spectrum Management, Channel Estimation, MIMO, Resource Allocation.

I. Introduction

Wireless communication systems have undergone tremendous transformation over the past three decades, enabling high-speed data transfer, low-latency applications, and massive device connectivity. Emerging technologies such as 5G, 6G, Massive MIMO, and Internet of Things (IoT) require highly adaptive and efficient systems capable of handling complex, dynamic environments. Traditional communication techniques rely heavily on analytical models and mathematical approximations. However, in real-world deployments, these models may not fully capture the non-linearities and uncertainties of the communication environment. Machine Learning offers an alternative, data-driven approach capable of learning from large datasets, predicting outcomes, and adapting to changing network conditions without explicit reprogramming. The integration of ML into wireless communication promises

significant improvements in network efficiency, spectral utilization, and overall quality of service (QoS).

II. Overview of Machine Learning in Communication Systems

Machine Learning techniques, particularly Supervised Learning, Unsupervised Learning, and Reinforcement Learning (RL), are being widely applied to various components of wireless systems.

- Supervised Learning: Used for tasks like channel estimation and modulation classification, where labeled data is available.
- Unsupervised Learning: Applied in clustering-based spectrum sensing and interference detection.
- Reinforcement Learning: Used for dynamic resource allocation and power control by interacting with the environment and learning optimal strategies.

The role of ML in different layers of wireless communication systems, from the physical layer to the application layer.

III. Applications of Machine Learning in Wireless Communication

A. Signal Detection and Channel Estimation

Accurate **channel estimation** is essential for coherent detection in wireless systems. Traditional methods such as **Least Squares (LS)** and **Minimum Mean Square Error (MMSE)** suffer performance degradation under non-linear channel conditions. ML-based estimators, such as Deep Neural Networks (DNNs) and Convolutional Neural Networks (CNNs), have demonstrated improved accuracy by learning non-linear mappings between received signals and transmitted data.

B. Spectrum Management

Efficient spectrum utilization is critical due to the limited availability of radio frequency resources. ML enables **dynamic spectrum access (DSA)** by predicting spectrum occupancy patterns and enabling secondary users to utilize underused frequency bands without interfering with primary users. Techniques like Support Vector Machines (SVM) and Long Short-Term Memory (LSTM) networks have shown promising results in spectrum prediction.

C. Beamforming in Massive MIMO Systems

Massive MIMO requires precise beamforming to direct signals toward specific users while minimizing interference. Traditional algorithms rely on perfect channel state information (CSI), which is often unavailable. ML models can learn from historical CSI data to predict beamforming vectors in real-time, reducing computational complexity.

D. Resource Allocation and Power Control

Efficient resource allocation ensures optimal network performance and energy efficiency. Reinforcement Learning (RL) methods like Q-learning and Deep Q-Networks (DQN) can dynamically allocate bandwidth, assign users to base stations, and control transmission power to optimize network throughput and minimize interference.

E. Error Correction and Modulation Classification

ML models can enhance error correction by predicting error patterns in noisy environments. Moreover, modulation classification, essential for cognitive radio systems, benefits from supervised learning methods that classify modulation schemes with high accuracy under low SNR conditions.

IV. Challenges in Integrating ML with Wireless Systems

Despite its potential, integrating ML into wireless communication faces several challenges:

1. Data Availability and Quality: Obtaining high-quality labeled data for training is difficult in dynamic environments.
2. Real-Time Processing: Many ML models are computationally intensive, making real-time deployment challenging.
3. Model Generalization: ML models trained on specific environments may not generalize well to other network conditions.
4. Security Concerns: ML models can be vulnerable to adversarial attacks that manipulate input data.
5. Energy Consumption: Running complex ML algorithms on low-power devices can drain battery life.

V. Future Research Directions

Future research should focus on:

- Federated Learning (FL) for privacy-preserving, distributed model training.
- Explainable AI (XAI) to make ML models more interpretable for network engineers.
- Green AI to develop energy-efficient ML algorithms.
- Hybrid ML-Analytical Models that combine the accuracy of ML with the interpretability of traditional methods.
- 6G-Ready ML Models optimized for ultra-reliable low-latency communication (URLLC) and AI-native networks.

VI. Conclusion

Machine Learning has the potential to revolutionize wireless communication systems by enabling intelligent, adaptive, and efficient network operations. Its applications in channel estimation, spectrum management, beamforming, and resource allocation can significantly enhance performance in next-generation networks. However, challenges such as data scarcity, real-time deployment, and security need to be addressed for large-scale adoption. The synergy between ML and wireless communication will play a pivotal role in shaping the future of 6G and beyond.

References

[1] T. O'Shea and J. Hoydis, "An Introuction to Deep Learning for the Physical Layer," IEEE Trans. Cogn. Commun. Netw., vol. 3, no. 4, pp. 563–575, Dec. 2017.

[2] C. Zhang, P. Patras, and H. Haddadi, "Deep Learning in Mobile and Wireless Networking: A Survey," IEEE Commun. Surveys Tuts., vol. 21, no. 3, pp. 2224–2287, 2019.

[3] M. Chen, U. Challita, W. Saad, C. Yin, and M. Debbah, "Artificial Neural Networks for Wireless Networks: Techniques, Applications, and Future Directions," IEEE Commun. Mag., vol. 55, no. 9, pp. 18–25, Sept. 2017.

[4] S. Huang, X. Liu, and Z. Ding, "Deep Learning-Based Modulation Recognition for Wireless Communications," IEEE Trans. Veh. Technol., vol. 67, no. 11, pp. 10760–10769, Nov. 2018.

[5] Y. Sun, M. Peng, Y. Zhou, Y. Huang, and S. Mao, "Application of Machine Learning in Wireless Networks: Key Techniques and Open Issues," IEEE Commun. Surveys Tuts., vol. 21, no. 4, pp. 3072–3108, 2019.

[6] H. Ye, G. Y. Li, and B.-H. Juang, "Power of Deep Learning for Channel Estimation and Signal Detection in OFDM Systems," IEEE Wireless Commun. Lett., vol. 7, no. 1, pp. 114–117, Feb. 2018.

[7] X. Wang, Y. Han, V. C. M. Leung, D. Niyato, X. Yan, and X. Chen, "Convergence of Edge Computing and Deep Learning: A Comprehensive Survey," IEEE Commun. Surveys Tuts., vol. 22, no. 2, pp. 869–904, 2020.

[8] M. Mahmood, H. Jamal, and S. Rehman, "Machine Learning Based Dynamic Spectrum Access in Cognitive Radio Networks," IEEE Access, vol. 8, pp. 85132–85143, 2020.

[9] F. Tang, Y. Kawamoto, N. Kato, and J. Liu, "Future Intelligent and Secure Vehicular Network Toward 6G: Machine-Learning Approaches," Proc. IEEE, vol. 108, no. 2, pp. 292–307, Feb. 2020.

[10] M. Elsayed and M. Erol-Kantarci, "AI-Enabled Future Wireless Networks: Challenges, Opportunities, and Open Issues," IEEE Veh. Technol. Mag., vol. 14, no. 3, pp. 70–77, Sept. 2019.

Internet of Things (IoT) in Communication Networks: Challenges and Solutions

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Abstract: The Internet of Things (IoT) is revolutionizing communication networks by enabling the interconnection of billions of devices, sensors, and systems across diverse domains such as healthcare, transportation, manufacturing, and smart cities. IoT-based communication networks must support massive device connectivity, low latency, high energy efficiency, and robust security. However, the integration of IoT into existing and future communication infrastructures presents several challenges, including interoperability, scalability, spectrum management, and cybersecurity threats. This paper presents an overview of IoT in communication networks, identifies major challenges, and discusses potential solutions involving advanced communication technologies, standardization efforts, and artificial intelligence-based optimizations.

I. Introduction

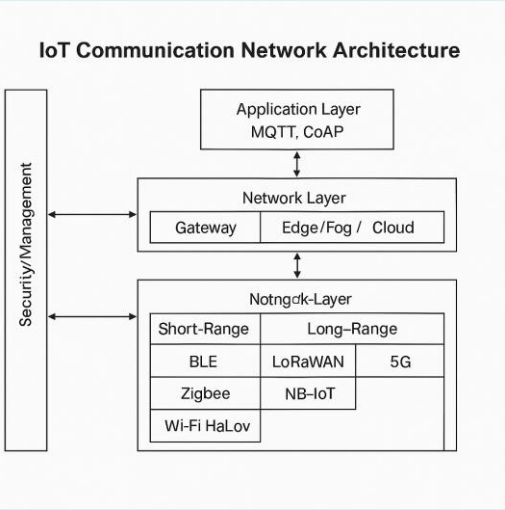

Fig. 1: Illustrates a simplified IoT communication network architecture integrating edge, fog, and cloud computing for efficient data processing.

The Internet of Things (IoT) refers to the network of physical devices embedded with sensors, actuators, and communication capabilities, enabling them to collect, exchange, and act upon data without human intervention. It is estimated that over

25 billion IoT devices will be deployed by 2030, driving demand for scalable and efficient communication networks. IoT communication networks span various layers, from short-range technologies like Bluetooth and Zigbee to long-range solutions like LoRaWAN, NB-IoT, and 5G. With the growth of applications such as smart healthcare, intelligent transportation, and industrial automation, IoT networks are becoming increasingly complex.

II. IoT Communication Network Architecture

A typical IoT communication network consists of:

1. Perception Layer — Includes sensors and devices for data acquisition.
2. Network Layer — Transports data using protocols such as Wi-Fi, LTE-M, NB-IoT, Zigbee, and LoRa.
3. Application Layer — Interfaces with end-users, providing services like smart home control, environmental monitoring, and predictive maintenance.

Fig. 1 illustrates a simplified IoT communication network architecture integrating edge, fog, and cloud computing for efficient data processing.

III. Communication Technologies for IoT

A. Short-Range Communication

- Bluetooth Low Energy (BLE): Low power consumption, ideal for wearable devices.
- Zigbee: Mesh networking for home automation and industrial monitoring.
- Wi-Fi HaLow: Low-power, long-range Wi-Fi standard for IoT.

B. Long-Range Communication

- LoRaWAN: Low-power wide-area network with long-range capabilities.
- NB-IoT: Licensed spectrum LPWAN optimized for deep indoor coverage.
- 5G IoT: Ultra-reliable low-latency communication (URLLC) for mission-critical applications.

IV. Challenges in IoT Communication Networks

A. Interoperability

Multiple standards and proprietary solutions hinder seamless device communication.

B. Scalability

As device density increases, networks face congestion, high latency, and resource allocation issues.

C. Spectrum Management

The limited availability of spectrum requires efficient allocation methods to avoid interference.

D. Energy Efficiency

Battery-powered IoT devices require ultra-low-power communication protocols.

E. Security and Privacy

IoT devices are vulnerable to cyber-attacks such as Distributed Denial of Service (DDoS), man-in-the-middle attacks, and data breaches.

V. Solutions to IoT Communication Challenges

A. Standardization and Interoperability Frameworksa

Efforts such as **OneM2M** and **IEEE P2413** aim to develop unified IoT architectures.

B. Edge and Fog Computing

Reduces latency by processing data closer to the device, minimizing cloud dependency.

C. AI-Driven Network Management

Machine learning algorithms can optimize spectrum allocation, predict network congestion, and enhance QoS.

D. Blockchain for IoT Security

Blockchain provides decentralized authentication, integrity verification, and secure device-to-device communication.

E. Energy Harvesting Technologies

Techniques such as solar, RF energy harvesting, and piezoelectric generation can prolong device lifetime.

VI. Future Directions

The convergence of IoT with 6G communication networks will enable:

- AI-native IoT devices with autonomous decision-making.
- Integration of Terahertz communication for ultra-high data rates.
- Digital twins for real-time simulation of IoT systems.
- Quantum communication for enhanced security.

VII. Conclusion

The Internet of Things is transforming communication networks, enabling smart and connected environments. However, IoT deployment at scale faces challenges in interoperability, scalability, spectrum management, and security. Emerging

solutions, including standardization, AI-driven management, blockchain, and energy harvesting, are paving the way for resilient and efficient IoT communication infrastructures.

References

[1] L. Atzori, A. Iera, and G. Morabito, "The Internet of Things: A Survey," Computer Networks, vol. 54, no. 15, pp. 2787–2805, Oct. 2010.

[2] F. A. Alaba, M. Othman, I. A. T. Hashem, and F. Alotaibi, "Internet of Things Security: A Survey," J. Netw. Comput. Appl., vol. 88, pp. 10–28, June 2017.

[3] M. R. Palattella et al., "Internet of Things in the 5G Era: Enablers, Architecture, and Business Models," IEEE J. Sel. Areas Commun., vol. 34, no. 3, pp. 510–527, Mar. 2016.

[4] A. Zanella, N. Bui, A. Castellani, L. Vangelista, and M. Zorzi, "Internet of Things for Smart Cities," IEEE Internet Things J., vol. 1, no. 1, pp. 22–32, Feb. 2014.

[5] H. Ning and H. Liu, "Cyber-Physical-Social Based Security Architecture for Future IoT," Adv. Internet Things, vol. 2, no. 1, pp. 1–7, Feb. 2012.

[6] M. Centenaro, L. Vangelista, A. Zanella, and M. Zorzi, "Long-Range Communications in Unlicensed Bands: The Rising Stars in the IoT and Smart City Scenarios," IEEE Wireless Commun., vol. 23, no. 5, pp. 60–67, Oct. 2016.

[7] J. Gubbi, R. Buyya, S. Marusic, and M. Palaniswami, "Internet of Things (IoT): A Vision, Architectural Elements, and Future Directions," Future Gener. Comput. Syst., vol. 29, no. 7, pp. 1645–1660, Sept. 2013.

[8] Y. Mao, C. You, J. Zhang, K. Huang, and K. B. Letaief, "A Survey on Mobile Edge Computing: The Communication Perspective," IEEE Commun. Surveys Tuts., vol. 19, no. 4, pp. 2322–2358, 2017.

[9] K. Christidis and M. Devetsikiotis, "Blockchains and Smart Contracts for the Internet of Things," IEEE Access, vol. 4, pp. 2292–2303, 2016.

[10] Z. Zhang, Y. Xiao, Z. Ma, M. Xiao, Z. Ding, X. Lei, G. K. Karagiannidis, and P. Fan, "6G Wireless Networks: Vision, Requirements, Architecture, and Key Technologies," IEEE Veh. Technol. Mag., vol. 14, no. 3, pp. 28–41, Sept. 2019.

Optimizing Embedded Systems for Performance and Power Efficiency

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Abstract: Embedded systems are specialized computing platforms designed to perform dedicated functions with constraints on performance, size, cost, and energy consumption. With the increasing deployment of embedded systems in Internet of Things (IoT) devices, automotive electronics, medical devices, and industrial automation, optimizing both performance and power efficiency has become a critical design challenge. This article explores the key techniques, architectures, and methodologies used to achieve this optimization.

1. Introduction

Performance and power efficiency are often at odds in embedded systems. High performance generally demands more processing power and energy, while power-constrained applications require designers to trade off speed and computational capacity for longer battery life or lower energy budgets. Optimization must therefore consider both hardware and software components, leveraging holistic design strategies that span the entire system stack.

2. Hardware-Level Optimization

2.1 Processor Architectures

Low-power microcontroller units (MCUs), such as ARM Cortex-M and RISC-V cores, are commonly used in embedded systems. These architectures support several features aimed at optimizing energy efficiency:

- **Dynamic Voltage and Frequency Scaling (DVFS):** Adjusts the processor's voltage and frequency in real-time to match workload demands, reducing power consumption during idle or low-activity periods [1].
- **Clock Gating:** Shuts off the clock signal to inactive components to save dynamic power [2].

- **Multiple Power Domains:** Allows selective powering of different parts of the system, reducing leakage currents.

2.2 Specialized Accelerators

Integrating application-specific integrated circuits (ASICs) or field-programmable gate arrays (FPGAs) to offload computationally intensive tasks can significantly enhance performance while maintaining energy efficiency. Examples include digital signal processors (DSPs) for audio processing or hardware accelerators for cryptographic operations [3].

3. Software-Level Optimization

3.1 Compiler Techniques

Compilers can play a crucial role in optimizing embedded applications through:

- **Loop unrolling and function inlining:** Reduces overhead but must be carefully managed to avoid code bloat.
- **Instruction scheduling and register allocation:** Minimizes memory access and enhances instruction-level parallelism [4].

Compiler flags like `-Os` (optimize for size) and `-O2`/`-O3` (optimize for speed) allow developers to target specific goals during compilation.

3.2 Real-Time Operating Systems (RTOS)

RTOS platforms like FreeRTOS or Zephyr provide efficient task scheduling and inter-process communication mechanisms. Using an RTOS enables:

- **Predictable timing behavior** for real-time tasks.
- **Idle-time power management** via sleep modes when no tasks are running [5].

4. Power Management Techniques

4.1 Sleep Modes and Wake-Up Strategies

Most modern embedded MCUs offer multiple sleep modes, such as:

- **Idle Mode:** CPU stopped peripherals active.

- **Standby Mode:** Minimal power use, quick wake-up.
- **Deep Sleep Mode:** Most components powered down, longest wake-up time.

Effective power management includes carefully timing transitions between these modes based on system activity patterns [6].

4.2 Energy Harvesting and Battery Management

In energy-constrained environments (e.g., remote sensors), energy harvesting from solar, thermal, or vibrational sources can extend system lifetime. Power management ICs (PMICs) and battery fuel gauges optimize charging and usage cycles [7].

5. System-Level Design Approaches

5.1 Hardware-Software Co-Design

Collaborative development of hardware and software components ensures that system-level constraints are met. For example, a software algorithm can be restructured to fit into a smaller cache or use fixed-point arithmetic instead of floating-point, reducing power consumption without degrading functionality [8].

5.2 Modelling and Simulation

Tools like MATLAB/Simulink, SystemC, and power estimation frameworks allow designers to simulate different configurations and choose optimal trade-offs between power and performance before fabrication or deployment.

6. Case Study: Low-Power IoT Sensor Node

Consider an IoT sensor node tasked with periodic data collection and wireless transmission. Power-efficient design includes:

- Using an ultra-low-power MCU (e.g., TI MSP430).
- Sampling data in burst mode and processing it locally.
- Transmitting compressed data via low-power radio (e.g., LoRa).
- Entering deep sleep between data collection intervals.

Such a node can operate for months or years on a coin-cell battery, demonstrating the impact of optimized design.

7. Conclusion

Optimizing embedded systems for performance and power efficiency is a multifaceted challenge involving processor selection, power management, software optimization, and system-level design. As embedded devices continue to proliferate in all aspects of modern life, energy-aware design is becoming not only a best practice but a necessity.

References

[1] Tiwari, V., Malik, S., & Wolfe, A. (1994). Power analysis of embedded software: A first step towards software power minimization. IEEE Transactions on VLSI Systems.

[2] Benini, L., Micheli, G. D. (2000). System-level power optimization: Techniques and tools. ACM Transactions on Design Automation of Electronic Systems.

[3] Wolf, W. (2001). Modern VLSI Design: IP-Based Design. Prentice Hall.

[4] Muchnick, S. S. (1997). Advanced Compiler Design and Implementation. Morgan Kaufmann.

[5] Yiu, J. (2015). The Definitive Guide to ARM® Cortex®-M3 and Cortex®-M4 Processors. Newnes.

[6] Texas Instruments. (2019). Low Power Modes in MSP430 Microcontrollers [Application Note].

[7] Roundy, S., Wright, P. K., & Rabaey, J. (2003). A study of low level vibrations as a power source for wireless sensor nodes. Computer Communications.

[8] Gajski, D., et al. (1994). Hardware/Software Co-design: Principles and Practice. Springer.

Adaptive beamforming and its applications

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Adaptive beamforming is a signal processing technique that dynamically adjusts antenna array weights to enhance desired signal reception while suppressing interference and noise. This article explores its principles, applications, and recent advancements, focusing on robustness in non-Gaussian noise environments.

Fundamentals of Adaptive Beamforming

Adaptive beamforming optimizes the **Signal-to-Interference-plus-Noise Ratio (SINR)** by adjusting complex weights across an antenna array. For an *N*-element array, the output signal is [1]:

$$y(k) = \mathbf{w}^H \mathbf{x}(k)$$

where $\mathbf{w}$ is the weight vector, and $\mathbf{x}(k)$ combines the desired signal, interference, and noise[1]. Traditional algorithms like **Least Mean Squares (LMS)** and **Recursive Least Squares (RLS)** minimize mean square error (MSE) but perform poorly under **impulsive noise** due to reliance on second-order statistics[1].

Applications

1. **Wireless Communications**:
    - Enhances signal quality in 5G/6G networks by focusing beams toward users.
    - Mitigates multi-path interference in urban environments.
2. **Radar and Sonar Systems**:
    - Improves target detection by steering nulls toward jammers.
    - Used in phased-array radars for real-time tracking.
3. **Microphone Arrays**:
    - Isolates speech signals in noisy environments (e.g., conferencing systems).

4. **Satellite Communications**:
    - Compensates for signal fading caused by atmospheric disturbances.

Challenges in Non-Gaussian Noise

Conventional beamformers assume Gaussian noise, but real-world environments often exhibit **impulsive noise** (e.g., lightning, machinery). This degrades performance, as MSE-based methods are sensitive to outliers[1].

Recent Advancements: CMCCC Algorithm

The **Constrained Maximum Complex Correntropy Criterion (CMCCC)** addresses non-Gaussian noise by leveraging **complex correntropy**, a high-order statistical measure robust to outliers [2].

Key Features

- **Complex Correntropy**: Measures similarity between complex variables using a Gaussian kernel [3]:

$$V_\sigma^C(C_1, C_2) = \mathbb{E}\left[\exp\left(-\frac{(C_1 - C_2)(C_1 - C_2)^*}{2\sigma^2}\right)\right]$$

- **Wirtinger Calculus**: Handles non-analytic cost functions for gradient computation [4].
- **Adaptive Weight Update**: Adjusts weights via steepest ascent:

$$\mathbf{w}_{n+1} = \mathbf{w}_n + \mu \frac{\partial J_{\text{CMCCC}}}{\partial \mathbf{w}^*} - \mathbf{C}\mu\lambda$$

Performance Comparison

Metric	CMCCC	CLMS	CAPA
Output SINR (dB)	15.2	9.8	11.5
Convergence Speed	Fast	Slow	Moderate

CMCCC achieves **55% higher SINR** than CLMS and **32% higher** than CAPA in impulsive noise [5].

Future Directions

1. **Real-Time Implementation**: Optimize computational complexity for embedded systems.
2. **6G Networks**: Integrate with reconfigurable intelligent surfaces (RIS) for enhanced coverage.
3. **Machine Learning**: Hybrid approaches combining CMCCC with deep learning for dynamic environments.

Conclusion

Adaptive beamforming is pivotal in modern signal processing, with CMCCC emerging as a robust solution for non-Gaussian noise. Its integration of complex correntropy and Wirtinger Calculus offers superior SINR and convergence, making it suitable for next-generation communication systems.

References-

[1] Van Trees, H.L.: Detection, estimation, and modulation theory, Optimum Array Processing, Hoboken, NJ. Wiley, USA (2004)

*[2] VanVeen,B.D., Buckley, K.M.:Beamforming: a versatile approach to spatial filtering. IEEE ASSP Mag. **5**(2), 4–24 (1988)*

*[3] Applebaum, S.: Adaptive arrays. IEEE Trans. Antennas Propag. **AP–24**(5), 585–598 (1976)*

*[4] Frost, O.L., III.: An algorithm for linearly constrained adaptive array processing. Proc. IEEE **60**(8), 926–935 (1972)*

*[5] Widrow, B., McCool, J.M., Larimore, M.G., Johnson, C.R.: Stationary and nonstationary learning characteristics of the LMS adaptive filter. Proc. IEEE **64**(8), 1151–1162 (1976)*

Klystrons: The Unsung Heroes of High- Frequency Power

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In the vast world of electronics, some devices quietly power our technologies without ever becoming household names. One such silent powerhouse is the klystron—a specialized vacuum tube responsible for amplifying high-frequency radio waves in radar systems, satellite communications, and even particle accelerators.

What is a Klystron?

A klystron is a linear-beam vacuum tube that amplifies microwave signals through the interaction of an electron beam with radio frequency (RF) fields. It was first invented in 1937 by American engineers Russell and Sigurd Varian, and since then, it has been a cornerstone in applications requiring extremely high power and stability.

How Does a Klystron Work?

At its heart, the klystron uses a stream of electrons that travel through cavity resonators— structures that allow RF energy to be exchanged efficiently. Here's how it works:

1. Electron Gun: Emits a focused beam of electrons.

2. Buncher Cavity: Introduces RF energy, causing electrons to speed up or slow down.

3. Drift Space: Allows the electrons to bunch together due to velocity differences.

4. Catcher Cavity: The bunched electrons pass through and transfer energy to the RF field.

5. Collector: Collects electrons after they've done their job.

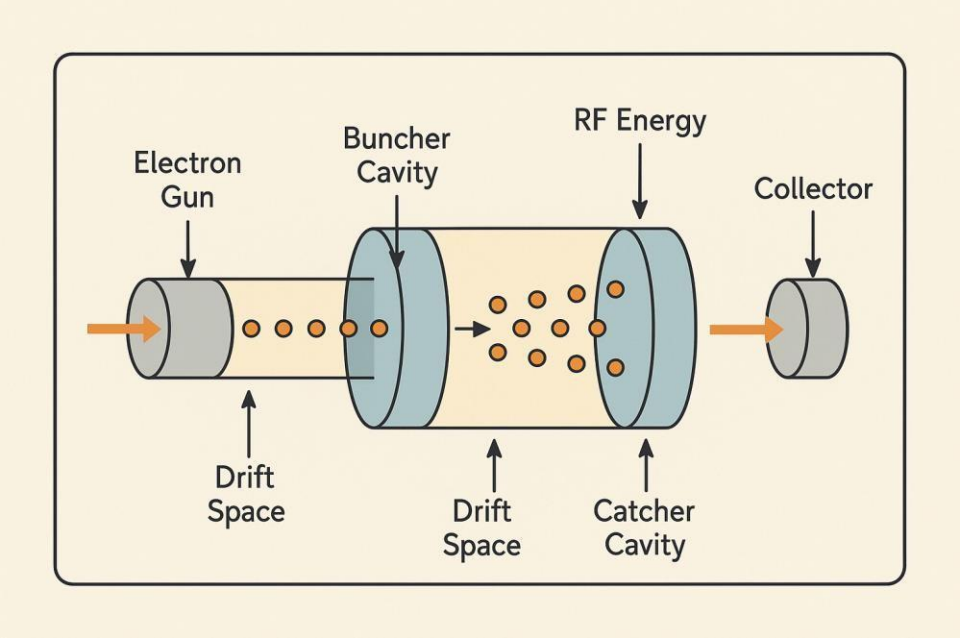

Figure 1: Simplified schematic showing the electron gun, resonant cavities, and collector.

Applications That Touch the Sky

- Klystrons are the backbone of numerous high-frequency systems:
- Radar Systems: For air traffic control and weather forecasting.
- Satellite Communication: High-power uplink signals.
- Television Broadcasting: Especially in UHF and microwave bands.
- Particle Accelerators: Driving the RF cavities to accelerate particles close to the speed of light.

While both are microwave amplifiers, klystrons are favored for high power and frequency stability, whereas TWTs offer broader bandwidth. Your choice depends on the application: precision or versatility.

Did You Know?

The name 'klystron' comes from the Greek word ‘kluzein’, meaning 'to wave,' and ‘tron’ a suffix used for instruments.

Figure 2: A high-power klystron used in satellite communication.

Final Thoughts

The klystron may not be as well-known as transistors or ICs, but it remains a critical part of modern communication and scientific exploration. It's a prime example of how deep engineering and physics power the technology behind our everyday conveniences.

References

[1] Varian, R., & Varian, S. (1939). A high frequency oscillator and amplifier. "Journal of Applied Physics", 10(5), 321-327.

[2] Gilmour, A. S. (2011). "Klystrons, Traveling Wave Tubes, Magnetrons, Crossed- Field Amplifiers, and Gyrotrons. Artech House.*

[3] Pozar, D. M. (2011). "Microwave Engineering" (4th ed.). Wiley.

[4] National Accelerator Laboratory. Klystrons in Particle Physics. Retrieved from https://www.fnal.gov

[5] NASA Technical Reports. Satellite Communications Using Klystrons. Retrieved from https://ntrs.nasa.gov

Analysis and Comparison of Compound Semiconductors in CS-DMG-JAM MOSFET Structures for High-Speed and Switching Applications

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INTRODUCTION

The aggressive scaling associated with device miniaturization has introduced a range of challenges, notably Short Channel Effects (SCEs) and Hot Carrier Effects (HCEs) [1–3]. To mitigate these issues, a variety of multiple-gate device architectures were developed [4–6], among which the Gate-All-Around (GAA) configuration emerged as particularly effective due to its exceptional electrostatic control over the channel. Despite its advantages, the GAA structure presents a significant drawback — the abrupt formation of source/drain junctions. This problem was effectively addressed with the introduction of the Junctionless Transistor (JLT) [7], which utilizes uniform doping throughout the device, thereby eliminating the need for abrupt junctions.

JLTs offer several benefits, including simplified fabrication processes, reduced leakage currents, and enhanced scalability. However, they suffer from Carrier Mobility Degradation (CMD) due to the high doping concentrations [8]. To overcome this limitation, an improved structure known as the Junctionless Accumulation Mode (JAM) MOSFET was proposed [9– 10], which reduces the doping concentration in the channel relative to the source/drain regions, thereby alleviating CMD while retaining the core advantages of junctionless operation.The CS-DMG-JAM MOSFET [8], an advanced JAM-based structure, incorporates a cylindrical architecture with dual-metal gates having different work functions ($\phi1>\phi2$). While silicon is widely used in MOSFETs, III-V compound semiconductors [9, 10] like GaN, GaAs, and InP offer higher electron mobility and are promising alternatives for high- performance applications. CS-DMG-JAM MOSFET structure is being illustrated in Figure 1. Doping done throughout the MOSFET is of n-type, where the channel of length 50nm is moderately less doped than source/drain (n+-n-n+). The considered device consists of two metal gates,

gate1 and gate2 with work-functions $\phi 1$ and $\phi 2$ respectively (where, $\phi 1 > \phi 2$). Models employed in the course of ATLAS 3-D [11] simulation are elaborated in Table I.

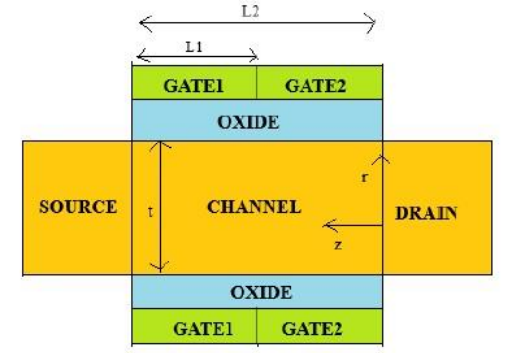

Fig. 1. Structural View of CS-DMG-JAM MOSFET

Table I Models Employed

Recombination Model	The SRH recombination model is incorporated to embrace the minority recombination effects.
Concentration Dependent Model	CONMOB connects the low-field mobility with the impurity concentration.
Field Dependent Mobility Model	FLDMOB associates the velocity saturation effect during the simulation process.
Statistics	Boltzmann Model to examine the Statistics
Methods	Newton and Gummel methods are called for the numerical solution at the same time.

The transfer characteristics (I_d vs. V_{gs}) illustrate the device's efficiency in conducting current. Figure 2 presents the transfer characteristics of the CS-DMG-JAM MOSFET for various compound semiconductors (GaN, GaAs, InP) and silicon (Si) at V_{ds} = 0.1V. It is evident from the figure that the GaN-based MOSFET delivers a significantly higher drain current compared to the other materials. Consequently, GaN-based devices are more suitable for high-current applications. Figure 3 shows the output characteristics (I_d vs. V_{ds}) for the device with different semiconductor materials. As observed in Figure 3, the GaN-based device consistently exhibits higher drain current, which can be credited to its wide

bandgap aand high saturation velocity [12, 13]. Therefore, the GaN-based CS-DMG-JAM MOSFET is highly advantageous for high-speed applications.

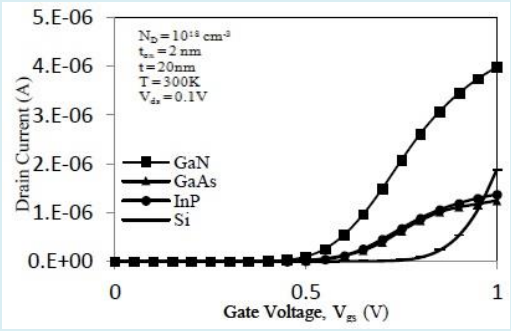

Fig. 2: Transfer characteristics for DM-JAM-CSG MOSFET considering different compound semiconductors (GaN, GaAs, InP) and Si.

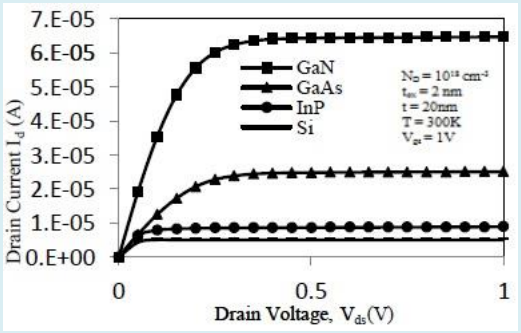

Fig. 3: Output characteristics for CS-DMG-JAM MOSFET considering different compound semiconductors (GaN, GaAs, InP) and Si.

Transconductance, gm [14] and output conductance, gd are crucial parameters for amplification applications and are given by:

$$g_m = (\Delta I_d / \Delta V_{gs})|V_{ds} = constant \quad (1)$$

$$g_d = (\Delta I_d / \Delta V_{ds})|V_{gs} = constant \quad (2)$$

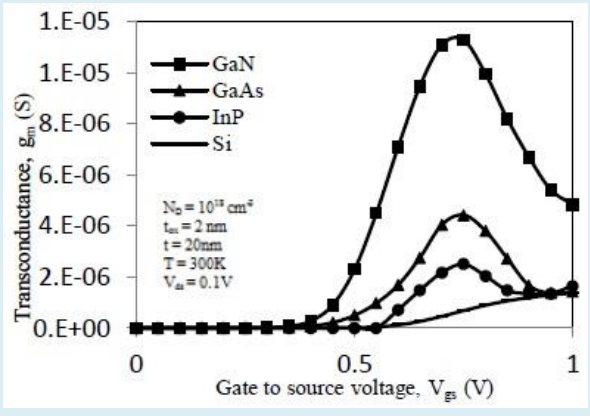

Fig. 4. Transconductance for CS-DMG-JAM MOSFET for various compound semiconductors (GaN, GaAs, InP) and Si.

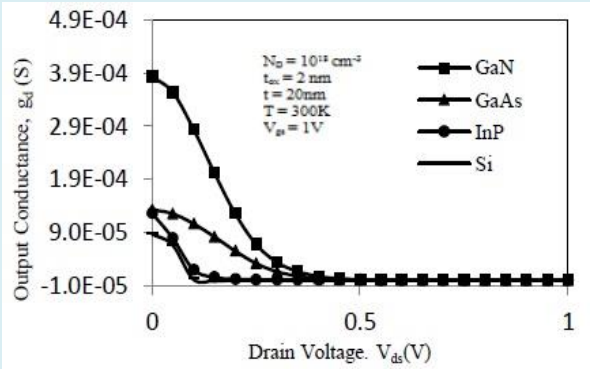

Fig.5. Output Conductance for CS-DMG-JAM MOSFET for different compound semiconductors (GaN, GaAs, InP) and Si.

GaN-based devices show higher *gm* and *gd*, making them suitable for high-gain circuits. This augmented output conductance is because of the higher drain current obtained for GaN- based MOSFET in comparison to others. Maximum Transfer Power Gain (MTPG) refers to the amount of power delivered to the load relative to the maximum power available from the source. Figure 6 illustrates the MTPG for the CS-DMG-JAM MOSFET device utilizing different semiconductors: GaN, GaAs, InP, and Si. Among these, GaN demonstrates the highest MTPG, thereby providing the greatest voltage gain. The cut-off frequency [15] is defined as

$$f_C = \frac{g_m}{2\pi C_{GG}} \qquad (3)$$

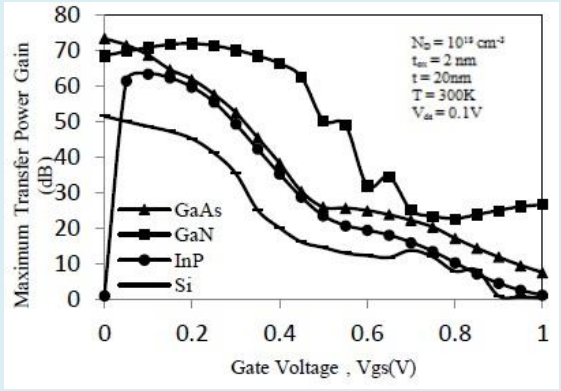

Fig. 6. Maximum Transfer Power Gain curve for CS-DMG- JAMMOSFET considering different compound.

where C_{GG} represents the gate capacitance. This parameter determines whether the device is suitable for high- or low-frequency applications. Figure 7 shows the cut-off frequency for the CS-DMG-JAM MOSFET using different semiconductors (GaN, GaAs, InP, and Si).

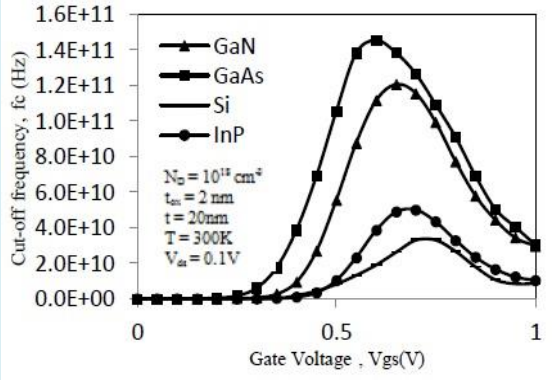

Fig. 7. Variation of cut-off frequency for CS-DMG-JAM MOSFETconsidering different compound semiconductors and Si.

Among all compound semiconductors and silicon-based MOSFETs, GaN exhibits the highest cut-off frequency. The superior peak cut-off frequency of GaN confirms its suitability for high- frequency applications.

CONCLUSION

The study establishes GaN as the optimal semiconductor material for CS-DMG-JAM MOSFETs in high-frequency, high-gain, and fast-switching applications. While manufacturing costs remain a challenge, ongoing research aims to make GaN more cost- effective, paving the way for its adoption in industries like telecommunications, power electronics, and aerospace. Future work should focus on reliability testing under extreme conditions and hybrid integration with silicon circuits to balance performance with cost- effectiveness.

REFERENCES

[1] Chaudhry, A., & Kumar, M. J. (2004). Controlling short-channel effects in deep-submicron SOI MOSFETs for improved reliability: a review. IEEE Transactions on Device and Materials Reliability, 4(1), 99-109.

[2] Xie, Q., Lee, C. J., Xu, J., Wann, C., Sun, J. Y. C., & Taur, Y. (2013). Comprehensive analysis of short-channel effects in ultrathin SOI MOSFETs. IEEE Transactions on Electron Devices, 60(6), 1814-1819.

[3] Oh, S. H., Monroe, D., & Hergenrother, J. M. (2000). Analytic description of short-channel effects in fully-depleted double-gate and cylindrical, surrounding-gate MOSFETs. IEEE electron device letters, 21(9), 445-447.

[4] Lee, C. W., Afzalian, A., Akhavan, N. D., Yan, R., Ferain, I., & Colinge, J. P.

(2009). Junctionless multigate field-effect transistor. Applied Physics Letters, 94(5), 053511.

[5] Pratap, Yogesh, Subhasis Haldar, R. S. Gupta, and Mridula Gupta. "Performance evaluation and reliability issues of junctionless CSG MOSFET for RFIC design." IEEE Transactions on Device and Materials Reliability 14, no. 1 (2014): 418-425.

[6] Kim, T. K., Kim, D. H., Yoon, Y. G., Moon, J. M., Hwang, B. W., Moon, D. I., ... & Lee, S. H. (2013). First demonstration of junctionless accumulation-mode bulk FinFETs with robust junction isolation. IEEE electron device letters, 34(12), 1479-1481.

[7] Holtij, T., Graef, M., Hain, F. M., Kloes, A., & Iñíguez, B. (2013). Compact model for short-channel junctionless accumulation mode double gate MOSFETs. IEEE Transactions on Electron Devices, 61(2), 288-299.

[8] Gupta, S., Pandey, N., & Gupta, R. S. (2020, December). Investigation of dual-material double gate junctionless accumulation- mode cylindrical gate all around (DMDG-JLAM-CGAA) MOSFET with High-k gate stack for low power digital applications. In 2020 IEEE 17th India council international conference (INDICON) (pp. 1-4). IEEE.

[9] Hudgins, J. L., Simin, G. S., Santi, E., & Khan, M. A. (2003). An assessment of wide bandgap semiconductors for power devices. IEEE Transactions on power electronics, 18(3), 907-914.

[10] Millan, J., Godignon, P., Perpiñà, X., Pérez-Tomás, A., & Rebollo, J. (2013). A survey of wide bandgap power semiconductor devices. IEEE transactions on Power Electronics, 29(5), 2155-2163.

[11] ATLAS, D. S. (2015). Silvaco International. Santa Clara.

[12] Baliga, B. J. (2013). Gallium nitride devices for power electronic applications. Semiconductor Science and Technology, 28(7), 074011.

[13] Li, T., Mastro, M., & Dadgar, A. (Eds.). (2010). III–V compound semiconductors: integration with silicon-based microelectronics. CRC press.

[14] *Arora, N. D. (2012). MOSFET models for VLSI circuit simulation: theory and practice. Springer Science & Business Media.*

[15] *Passi, V., & Raskin, J. P. (2017). Review on analog/radio frequency performance of advanced silicon MOSFETs. Semiconductor Science and Technology, 32(12), 123004.*

Carbon Nanotubes for Analog and Digital Building Blocks: A Pathway to Next-Generation Nanoelectronics

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Abstract : Carbon nanotubes (CNTs), owing to their exceptional electrical, thermal, and mechanical properties, have emerged as a promising alternative to traditional silicon-based technologies. Their ability to function as both metallic interconnects and semiconducting channels makes them suitable for realizing high-performance analog and digital building blocks. This article explores the application of carbon nanotube field-effect transistors (CNFETs) in the design and implementation of analog and digital integrated circuits (ICs), highlighting key advantages, challenges, and recent developments.

1. Introduction

As silicon-based CMOS technology approaches its physical scaling limits, carbon-based nanomaterials, particularly CNTs, present a promising solution for continued advancement in nanoelectronics. Carbon nanotubes, essentially rolled-up sheets of graphene, can be either metallic or semiconducting depending on their chirality and diameter. This property allows them to be tailored for specific electronic applications.

2. Carbon Nanotube Field-Effect Transistors (CNFETs)

CNFETs exploit semiconducting single-walled carbon nanotubes (SWCNTs) as channel material. These devices demonstrate near-ballistic transport, high carrier mobility, and low off-state leakage current. CNFETs are categorized into two types:

- **Schottky-barrier CNFETs (SB-CNFETs)**: Rely on carrier injection through Schottky barriers at the source/drain junctions.

- **MOSFET-like CNFETs**: Use heavily doped CNTs or different metal work functions to minimize Schottky barriers and resemble conventional MOSFET behavior.

3. CNTs in Digital Building Blocks

3.1 Logic Gates: CNT-based logic gates (e.g., inverters, NAND, NOR) demonstrate high-speed operation and reduced power consumption. CNFET inverters exhibit excellent voltage transfer characteristics, high gain, and low delay, making them ideal for use in larger digital systems.

3.2 Arithmetic Units: Researchers have implemented adders, multipliers, and other arithmetic circuits using CNFETs, benefiting from the low parasitics and scalability of CNTs. Hybrid CMOS-CNFET architectures have also been explored to combine the maturity of CMOS with the performance benefits of CNTs.

3.3 Memory: Static and dynamic RAM cells using CNFETs show promise in reducing cell size and improving read/write speed due to better electrostatic control and low threshold voltages.

4. CNTs in Analog Building Blocks

4.1 Amplifiers: CNFET-based amplifiers such as common-source, differential, and operational amplifiers exhibit high gain-bandwidth products and excellent linearity. These advantages stem from the intrinsic high transconductance and low output conductance of CNFETs.

4.2 Current Mirrors and Sources: Analog circuits benefit from the high output resistance and low channel-length modulation effects in CNFETs, which enable accurate current mirrors and sources for biasing and reference generation.

4.3 Filters and Oscillators: CNT-based active filters and oscillators have been demonstrated with improved phase noise performance and frequency stability, crucial for communication systems.

5. Advantages of CNT-Based Circuits

- **High Speed and Low Power**: Due to near-ballistic transport and low capacitance.

- **Scalability**: CNTs support aggressive scaling beyond the 5 nm technology node.
- **Enhanced Linearity**: Ideal for precision analog applications.
- **CMOS Compatibility**: CNFETs can be fabricated using processes compatible with existing CMOS infrastructure.

6. Challenges and Research Directions

- **Manufacturing Variability**: Chirality control and precise placement of CNTs remain major challenges.
- **Integration Complexity**: Co-integration with existing silicon circuits requires advanced fabrication techniques.
- **Reliability and Yield**: High device-to-device variability and defect rates impact large-scale integration.

Ongoing research is focused on improving chirality sorting, aligning CNTs at scale, and developing design tools for CNT-based ICs.

7. Conclusion

Carbon nanotubes hold significant potential for revolutionizing the design of analog and digital building blocks. While technical hurdles remain, continuous advancements in synthesis, modeling, and integration are pushing CNT-based electronics closer to practical deployment in high-performance, low-power applications.